"MASSACHUSETTS MICROELECTRONICS CENTER

SECOND DETAILED PLAN 6-18-86"

SECOND DETAILED PLAN

(REVISED)

THE MASSACHUSETTS MICROELECTRONICS CENTER

EXECUTIVE SUMMARY

This is the Second Detailed Plan for the Massachusetts Microelectronics Center. It proposes to supplement the Center as described in the First Plan through the creation of a baseline, fast turn-around, custom CMOS (Complimentary Metal Oxide Semiconductor) Integrated Circuit Fabrication Facility. The Fabrication Facility will complement the two elements of the Center currently in operation: a VLSI (Very Large Scale Integration) CAD (Computer Aided Design) Network with seven university sites and a central location in Westborough; and the DSIPL (Distributed Semiconductor Instructional Process Laboratory) Element, a series of instructional laboratories on university campuses. The First Detailed Plan for the Center was approved by the Governor and the House and Senate Committees on Ways and Means in the late Summer of 1985.

This Second Detailed Plan requests that the State approve the creation of the baseline Fabrication Facility. Specifically, it is requested that the State authorize the expenditure of the approximately $13.5 million remaining from initial $20 million appropriation for the Center. This $13.5 million, together with industry contributions commitments received and to be received in support of the Fabrication Facility, will defray the total costs of constructing and equipping a baseline Integrated Circuit Fabrication Facility. The Center has satisfied the industry match requirement of the

enabling act: industry has donated in excess of $20.3 million in the form of cash and equipment to the Center. As of the date of the submission of this revised Second Detailed Plan, the Center must still secure approximately $1.38 million dollars in contributions to defray the total capital costs of the baseline facility. The Center intends to secure the needed contributions before the construction of the facility is completed.

The Massachusetts Microelectronics Center is designed to take full advantage of the strengths and resources available in the Commonwealth: the leading university system in electrical and computer engineering in the Western World, a burgeoning technology-based economy, and a State government fully cognizant of the close relationship between the two. A fully operational Center will provide to the nine public and private engineering colleges and universities of the Commonwealth a dedicated educational resource second to none. In its entirety, the three element Center will enable our institutions of higher education to provide for the first time a comprehensive educational experience in an area of science and technology education of paramount importance to the economy of our State and Nation: semiconductor and microelectronics technologies.

A compelling sense of urgency surrounds this Second Detailed Plan. The Fabrication Facility element of the Center is of most immediate importance to the engineering colleges and universities of Massachusetts. Its primary purpose is to

fabricate student-designed integrated circuits quickly and efficiently. The opportunity for a student to test and characterize a circuit of his or her own design is absolutely required for a comprehensive exposure to the complexities of semiconductor and microelectronics technologies. A real time laboratory experience is the identifying characteristic and essential element of every engineering program. Its absence from so critical an area of technology is of distressing consequence to our engineering universities. A captive semiconductor fabrication facility will further assist the universities to attract and develop qualified faculty and sponsor innovative research endeavors.

The support for the Fabrication Facility among industrial organizations is no less substantial. Increasingly, the success or failure of an industrial enterprise depends upon the degree to which advances in semiconductor technology can be harnessed in support of specific problems and applications. The need for individuals with a comprehensive background in silicon based technology is intensive and expanding. This need can not presently be met by the graduates of Massachusetts' colleges and universities. The current economic resurgence of the Commonwealth's economy is eloquent testimony to the importance of a pre-eminent system of technology based higher education. But it also teaches us an important lesson: we are in an intensely competitive worldwide economy which has inexorably come to be driven by technological innovation and fueled by well educated

and trained individuals. We act at our peril if we neglect to continuously reinvest in our university resources.

The Fabrication Facility is a particularly appropriate subject for an unprecendented government-industry-academia partnership. The complexity and capital cost of the Fabrication Facility are beyond even the collective resources of our institutions of higher education. The facility's physical structure must be built to exacting vibrational and ambient tolerances. The equipment of the Fabrication facility is expensive and sophisticated; its operational demands are severe. The participating universities have no reliable mechanism to secure the required real time laboratory experience in semiconductor design other than through a dedicated circuit fabrication capacity.

The engineering universities of Massachusetts and the many industrial concerns represented on the Center's Board of Directors, speaking with one voice, respectfully request permission to proceed with the lengthy process of constructing the Center's Integrated Circuit Fabrication Facility. In consideration of the eighteen (18) months required for construction and the demands of scheduling construction around the New England winters, failure to initiate the construction process by this Summer will delay operation of the facility to mid-1989 at the earliest. It is imperative that this dedicated

resource be available to the colleges and universities of the Commonwealth as soon as possible.

In addition to the baseline Fabrication Facility for which approval is requested, this Plan reviews the Center's proposals to augment the Fabrication Facility in future years if additional industry support and/or State funds are available. Proposals for augmentation include the addition of a mask making capacity and the inclusion of certain capacities considered desireable but not absolutely necessary for the baseline facility. This Plan does not request that the State approve any of the foregoing proposals for augmentation at this time.

Admittedly, the Fabrication Facility proposed in this Plan is an expensive proposition for the Commonwealth of Massachusetts. The Fabrication Facility is expensive to construct and costly to operate. Yet it will provide a crucial component to the Commonwealth's system of public higher education in an area of science and technology critical for the Massachusetts economy. We respectfully request your support and assistance.

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1.0 Introduction

Slightly less than four years ago, an informal association of dedicated State officials, industry leaders and representatives of many of the major public and private engineering institutions of higher education in the Commonwealth approached the Legislature with an unprecedented proposal for a Massachusetts Microelectronics Center.

They declared that in an area of science and technology education considered critical for the State's economic development - semiconductor and microelectronic technologies - our colleges and universities could no longer support the type and breadth of instructional and research activity required to satisfy the needs of industry for an educated workforce, the demands of our citizens for new and rewarding opportunities for employment and career development, and the interests of our universities in retaining their worldwide preeminence as centers for sophisticated technological instruction and innovation. They recited that the anticipated consequence of failing to respond to these disturbing developments was that the long term economic health of the Commonwealth would be placed in jeopardy.

They proposed as the Commonwealth's response a daring and comprehensive State, industry and university partnership built around a microelectronics educational facility. To consist of the scientific equipment, machinery and technical assistance

required to support advanced instruction and research in semiconductor technology, to be established and operated with financial and technical assistance provided by the parties to the partnership, and to be linked to and supportive of our institutions of higher learning, the proposal represented a dramatic departure from both customary State government economic development initiatives and traditional endeavors in the field of higher education.

The proponents of the Microelectronics Center admitted that many questions surrounding such a facility remained unanswered. Would industry support such a concept? Would our universities agree to work together on a project of such magnitude? How could one facility support a number of universities of different sizes, with varying missions and located throughout the State? There were no other models to point to. Massachusetts was asked to break new ground.

The Legislature responded as it has throughout the long history of this Commonwealth: it took that first, most challenging step. It created the Massachusetts Technology Park Corporation as a formal governmental body and provided a substantial capital fund for the effort and the operating funds necessary for planning and initial implementation. A Board of Directors was appointed with broad general representation from State government, industry, and the institutions of higher education.

That Board was directed to return to the Legislature with a detailed proposal for the Massachusetts Microelectronics Center. The proposal was to describe in detail the need for such a facility, its proposed activities, and its projected capital and operating costs. To defray a portion of the Center's capital costs and to otherwise ensure that the Center as proposed was consistent with the needs of industry and academia, it was required that the proposal for the Center include evidence of contributions from industry and academia in support of the Center's creation and operation. Specifically, the Legislature required that industry match the State's capital outlay contribution for the Center and that institutions of higher education participate in a comprehensive manner in the Center's operation.

Since the creation of the Massachusetts Technology Park Corporation its Board of Directors, as a group, through its committees and through countless hours of individual effort, has attempted to execute faithfully its charge. A general direction for the Center was established early and refined over a period of years. That direction for the Center finds its detailed expression in this document and in the First Detailed Plan for the Center. Specific educational objectives were established for the Center and its elements and facilities programs, operational plans and implementation schedules were developed. At the same time, the Board chose an executive director and a location for

the Center, both after prolonged periods of painstaking investigation.

The Corporation resolved favorably a substantial federal tax disincentive to industry contributions. Industry in Massachusetts and throughout the United States was canvassed for capital contributions. Participating institutions of higher education were requested to tighten their belts and prepare to make a significant investment in the Center's success. Extreme care was taken by the Board to balance its determination of the minimum educational objectives for the Center with its expectations of what the State could reasonably afford. During the entire planning process, meetings of the Board and its committees were open to the public and the staff made every effort to keep members of the Legislature informed as to the Center's progress.

The State provided substantial support to the Board in its efforts. Planning funds were supplied as requested and critical directors whose terms had expired were reappointed. A substantial discussion ensued regarding the issue of site selection, but the nature of that discussion was precisely what was intended by the Legislature in the creation of the Corporation's Board of Directors. It bears noting that soon after the Board's determination as to the Center's location the State expeditiously transfered the desired State real property parcel to the Corporation.

This Detailed Plan advances the proposition that the situation facing our institutions of higher education today in microelectronics technology, and by implication the problem confronting our developing industries and the Commonwealth itself, is no less severe than that which was observed almost three years ago. The provision of adequate instructional opportunities in semiconductor design and processing is simply beyond the capabilities of our colleges and universities.

This Plan proposes to add to the central facility of the Center in Westborough a captive Integrated Circuit Fabrication Facility. The Fabrication Facility is to guarantee that student designed integrated circuits will be manufactured and returned to the students in a time frame consistent with a comprehensive educational process. This Second Plan includes a significant level of government, industry and university cooperation.

The Plan for the Center would not have been possible without the combined assistance of a great number of individuals and institutions too numerous to mention here. Some, however, are particularly deserving of a formal review. The members of the Board of Directors of the Massachusetts Technology Park Corporation have given enormously of their time and abilities on behalf of the Center project. Without their uncompromising dedication, this Plan could not have been developed. The industry donors to the Center, are of substantial significance.

Their willingness to invest in this innovative enterprise is eloquent testimony to their commitment to the Commonwealth of Massachusetts.

The Massachusetts Legislature, which has patiently supported the Center project since its inception, has been critical. The assistance of Senate President, William M. Bulger, former Senate Ways and Means Chairman and now Congressman Chester G. Atkins, the present Chairman of the Senate Committee on Ways and Means, Patricia McGovern, and the present Chairman of the House Committee on Ways and Means, Richard Voke, has been particularly welcomed. Similarly, the support of the Executive Branch of Massachusetts State government, including foremost the support of Governor Michael S. Dukakis, Secretary for Administration Frank Keefe, Development Director Alden Raine, former Secretary of Ecomonic Affairs Evelyn Murphy and Secretary of Ecomonic Affairs Joseph Alviani has been greatly appreciated.

This Second Detailed Plan supplements the Center as described in the First Detailed Plan, dated 1 July 1985. Although appropriate reference is made herein to the Center as described in that First Plan, it is recommended that both the First and the Second Plans for the Center be read together. The Plan is proffered by the Board of Directors of the Massachusetts Technology Park Corporation in support of the creation of the Massachusetts Microelectronics Center and in satisfaction of the statutory planning requirements contained in Sections 6(a) to

(c), inclusive, of Chapter 40J of the Massachusetts General laws.

By way of introduction, Sections 2 and 3 provide a comprehensive overview and explanation for both the Massachusetts Technology Park Corporation and the Massachusetts Microelectronics Center. Section 4 presents a chronology of the planning process for the Massachusetts Microelectronics Center since the submission of the First Detailed Plan. Section 4 reviews as well the statutory planning requirements for an educational center of the Corporation contained in the above-referenced provisions of Chapter 40J of the Massachusetts General Laws.

Section 5 provides the required descriptive, budgetary, and benefit analysis materials concerning the Massachusetts Microelectronics Center as proposed in this Second Detailed Plan. Section 6 provides the required factual findings with regard to the Center and details the Center's contribution commitments. A conclusion is presented in Section 7. Section 8 contains a number of appendices to this Plan regarding facility design and construction matters and the Board of Directors of the Massachusetts Technology Park Corporation and includes a glossary of technical terms employed in this document.

2.0 The Massachusetts Technology Park Corporation

2.1 A Public Instrumentality

The Massachusetts Technology Park Corporation (the "Corporation") was established by an Act of the Massachusetts Legislature, Chapter 312 of the Acts of 1982, inserting Chapter 40J Section 1 et. seq. into the Massachusetts General Laws ("Chapter 40J" or "enabling act"). Its enabling act was subsequently amended by Chapter 451 of the Acts of 1982 and Chapter 32 of the Acts of 1983. In addition, Chapter 327 of the Acts of 1983 provided a capital outlay appropriation to the Corporation and Chapter 405 of the Acts of 1984 authorized a transfer of public real property to the Corporation.

Section 3 of Chapter 40J provides that the Corporation is a "body, politic and corporate," and further, that it is:

> a public instrumentality of the [C]ommonwealth and the exercise by the corporation of the powers conferred in this chapter shall be deemed and held to be the performance of an essential governmental function.

The Corporation is placed "within the Executive Office of Manpower Affairs," but in not subject to the control of that State cabinet office, or of any other State agency, except as provided by the enabling act.

Section 1 of Chapter 40J provides that the statutory purpose of the Corporation is to:

> establish and operate one or more educational centers containing design, fabrication and testing facilities and equipment for post-secondary academic and practical training programs urgently required to satisfy the education and employment needs of business and industry and the people of the [C]ommonwealth.

Section 6(b)(1) of Chapter 40J provides that:

> the basic purpose of this chapter is to provide for the establishment and operation of centers for the education of qualified persons in a developing technology.

Said Section 1 notes, in addition, that the purpose of the Corporation is a "public purpose for which public money may be expended."

The Corporation's creation was predicated upon certain findings of fact made by the Legislature in Section 1 of Chapter 40J. The Legislature therein observed that the ability of Massachusetts' institutions of higher education to provide "the most advanced education and training opportunities in emerging areas of science and technology" has been crucial to the economic

development of the Commonwealth. The Legislature observed further, however, that in recent years the costs associated with providing such opportunities in highly complex and rapidly developing areas of science and technology have become prohibitive to Massachusetts colleges and universities.

Section 1 of Chapter 40J recites that these observations are most distressingly accurate at present with regard to the field of semiconductor and microelectronic technologies, an area of extreme importance to the State's burgeoning high technology industry. The Legislature concluded Section 1 with the finding that the creation of a public corporation for the purpose of establishing and operating educational centers, with the support of business and industry and in conjunction with institutions of higher education, to provide advanced, state-of-the-art instructional opportunities in emerging areas of science and technology, particularly and in the first instance in the field of semiconductor and microelectronics technologies, was a proper and legitimate governmental activity.

The Corporation then is a publicly created administrative vehicle established to develop negotiated partnerships among State government, businesses and institutions of higher education for the public purpose of supporting economic development within the Commonwealth by increasing the instructional programs and research opportunities available in critical, emerging areas of science and technology.

2.2 Public Control of the Corporation

In addition to being created by the Legislature for public purposes, the Corporation is controlled by a publicly appointed Board of Directors, subject to substantial scrutiny and control over the exercise of its powers by the Legislature and certain agencies of the Executive Branch of Massachusetts State Government, and principally dependent upon the public appropriations process for its operating funds. Further, the Corporation is limited by the express terms of its enabling act to activities and applications of its funds which are consistent with its public purposes. The dimensions of this public control over the Corporation are discussed below.

Section 3 of Chapter 40J provides that the Corporation "shall be governed and its corporate powers exercised by a board of directors . . ." Said Section 3 of Chapter 40J specifies that the Board of Directors is to consist of twenty-three members, three of whom are public officials serving by virtue of their offices and twenty of whom are individuals appointed by the Governor of the Commonwealth. The three ex officio directors are the Secretary of Manpower Affairs, the Secretary for Administration and Finance and the Chancellor of the Board of Regents of Higher Education. The twenty gubernatorial appointees are to include eight chief executive officers or distinguished faculty members of postsecondary educational institutions, and

eight chief executive officers, chairpersons or chief engineers of businesses concerned with the design and manufacture of semiconductor or microelectronics components or products of another appropriate technology. A list of the members of the Board of Directors is containied herein in Section 8.3.

The ex officio members of the Board are full voting directors. The gubernatorial appointees serve for staggered five year terms and may be removed by the Governor for cause. Directors serve without compensation but may be reimbursed for "actual and necessary expenses incurred in the performance of [their] official duties."

In the furtherance of its corporate purposes, the Corporation is empowered pursuant to Section 4 of Chapter 40J to, among other powers: make rules and regulations for the management of its affairs; sue and be sued in its own name; plan, construct and operate educational centers within the meaning of Chapter 40J; charge participating educational institutions for the use of such educational centers; prepare, publish and distribute technical studies, reports, and bulletins; and "do any and all things necessary or convenient to carry out the purpose of its enabling act."

The Corporation's exercise of its key powers to create and operate educational centers is subject to comprehensive scrutiny and control by the Massachusetts Legislature. Section 6

of Chapter 40J requires the Corporation, before constructing a proposed center, to develop a plan and make certain findings of fact with regard thereto and to submit the same to the Governor, President of the Senate, the Speaker of the House of Representatives and the Chairmen of the Senate and House Committees on Ways and Means. Section 5 of Chapter 40J provides that no funds appropriated for the construction of a particular center may be credited to the Corporation:

> unless and until the plan and findings required pursuant to section 6 of this chapter have been received and approved in writing by the [H]ouse and [S]enate [C]ommittees on [W]ays and [M]eans.

Section 5 provides further that if, subsequent to the creation of a center, business and educational institutions fail to provide adequate support for a center to the Corporation pursuant to Section 6 (b)(4) of Chapter 40J, then the Board of Directors must so notify the Massachusetts General Court, "which may dissolve the Corporation and direct the dissolution of its assets or take such other action as it deems appropriate."

The Corporation is dependent upon direct appropriations of public funds by the Legislature. A capital outlay appropriation specific to a particular proposed educational center is required for its construction by the Corporation and periodic annual maintenance appropriations are to be necessary

for the Corporation to meet its expenses of administration and operation. Each appropriation request of the Corporation must be reviewed and approved by the Executive Office of Manpower Affairs, the Office of the Governor and the Legislature as a part of the normal budget process.

The Corporation is required to submit an annual report on its activities to the Massachusetts General Court pursuant to Section 8 of Chapter 40J. Section 9 of Chapter 40J provides that "the books and records of the Corporation shall be subject to an annual audit by the auditor of the Commonwealth." The Corporation's activities are subject to review by the Office of the Inspector General pursuant to the provisions of Section 3 of Chapter 40J and Chapter 12A of the Massachusetts General Laws. The fourth paragraph of Section 3 of Chapter 40J provides that Chapter 268A of the Massachusetts General Laws, governing the conduct of public officials and employees of the Commonwealth, applies to the Corporation. Pursuant to Section 1(q) of said Chapter 268A directors, officers and employees of the Corporation are "[S]tate employees" for the purposes of the Act.

The Corporation is a "public agency" within the meaning of Section 44A(1) of Chapter 149 of the Massachusetts General Laws concerning the requirements for public construction projects. Pursuant to Section 4(k) and 5 of Chapter 40J, the authority of the Corporation to invest monies pending disbursement is circumscribed by Sections 34, 38 and 38A of

Chapter 29 of Massachusetts General Laws, regarding the investment of public funds.

The Corporation is an "agency" of State government for the purposes of Chapter 30A of the Massachusetts General Laws, the State Administrative Procedure Act. The Corporation is further a "Governmental Body" under Section 11A of said Chapter 30A, and as such is subject to the Open Meeting Law under Section 11A 1/2 of said Chapter 30A. The employees of the Corporation, pursuant to section 3 of Chapter 40J, are not subject to the normal rules of classification and remuneration under Section 45, 46 and 52 of Chapter 30 nor to the Civil Service provisions under Chapter 31 of the Massachusetts General Laws.

2.3 The Powers of the Corporation

As above noted, the Corporation is charged with creating and operating "educational centers" designed to foster economic development within the Commonwealth by increasing the instructional programs and research opportunities available in certain emerging areas of science and technology considered important for the ecomonic development of the Commonwealth. An educational center is broadly defined by Chapter 40J as a facility, owned and operated by the Corporation, which contains the equipment, machinery and instructional and technical resources necessary to provide such postsecondary instructional and research opportunites.

The Corporation's enabling act is reasonably precise in establishing standards with regard to the Corporation's exercise of its power to create an educational center. By statutory prescription, the first educational center of the Corporation is to be a facility concerned with the field of semiconductor and microelectronics technologies, to be known as the Massachusetts Microelectronics Center. Pursuant to Section 1 of Chapter 40J, the Corporation is empowered "to establish further similar centers to support . . . other technologies . . . where a need is found to exist similar to the current need for the Massachusetts Microelectronics Center."

Section 6 of Chapter 40J further circumscribes the Corporation's authority to establish educational centers. This Section provides that the Corporation must first develop a detailed descriptive plan for a proposed center and make certain findings of fact with regard thereto. The findings of fact required by Section 6(b) include findings that the proposed center is consistent with the economic development interests of the Commonwealth; that it will supplement and not duplicate the activities of traditional institutions of higher education in Massachusetts; and that it is beyond the financial means of any single college, university or consortium of the same in the Commonwealth. A critical finding of fact, required by Section 6(b)(4), is that:

> The corporation has received appropriate commitments from participating businesses and participating institutions to support the center . . .

The support from business and industry is required to include the equipment and machinery necessary to create and maintain a center at a level consistent with developing technology, provided that the support contributed to create a center must be equivalent in value to the State's capital outlay contribution. Further, the Corporation is required to find that both business and industry and educational institutions have agreed to provide "loaned instructors" to a center. Only after the submission of such plan and findings of fact by the Corporation to designated State officials pursuant to Section 6(c) of Chapter 40J, and the approval thereof pursuant to Section 5 of Chapter 40J, is the Corporation authorized to create an educational center.

In contrast to the carefully delineated authority of the Corporation to create an education center, the Corporation has been delegated a broad discretionary authority to operate a constitutent center. Section 1 of Chapter 40J expansively provides that the purpose of the Corporation is to "operate . . educational centers . . . for post secondary academic and practical training programs," while Section 4(t) of said Chapter empowers the Corporation "to do any and all things necessary or convenient to carry out the purposes of this Chapter." The expansive operating authority of the Corporation is necessary for

the Corporation to develop the negotiated partnerships which are integral to its statutory purpose. By definition, the terms of such partnerships, and hence the terms of operation of a particular educational center, are to be the subject of negotiation among the parties represented on the Board of Directors of the Corporation and are not amenable to advance strict statutory prescription. The enabling act, however, does provide general guidelines regarding the exercise by the Board of Directors of this broad operating authority.

Section 3 of Chapter 312 of the Acts of 1982 provides that:

> It is intended that the corporation established pursuant to the provisions of this chapter shall be an educational organization as described in 26 U.S.C. 170(b)(1)(A)(ii) and an institution of higher education as defined in 26 U.S.C. 3304(f).

In addition, Section 1 of Chapter 40J establishes that an important activity of the Corporation in discharging its statutory responsibility to function as an "educational organization" and an "institution of higher education" is to operate in conjunction with existing institutions of higher education in Massachusetts. The fourth paragraph thereof, in listing the "governmental functions" which the Corporation is intended to serve, provides as follows:

> to increase opportunities for gainful employment of our people, to assist in promoting a productive and expanding industrial base within the [C]ommonwealth capable of meeting the needs and demands of modern economy, [and] <u>to assist post-secondary educational institutions to assume an active role in achieving these goals</u>. (emphasis supplied)

Hence, in operating its constituent educational centers, the Corporation is initially constrained to follow two major statutory prescriptions: (i) the Corporation should operate its educational centers in a manner consistent with the above-referenced definitions of an "educational organization" and an "institution of higher education" and (ii) the Corporation should operate its educational centers in conjunction with interested Massachusetts' institutions of higher education.

Only activities of the Corporation with regard to an educational which are so incorporated in the detailed plan approved by the Governor and the Legislative leadership are within the power of the Corporation to support. In this regard, certain of the findings of fact which the Board of Directors is required to make and include in its detailed plan for an educational center serve to further illustrate the nature and scope of the Corporation's function.

Section 6(b)(2) of Chapter 40J requires the Board of Directors to find that:

> there is no reasonable expectation that the center as proposed in the plan will duplicate the actual or proposed facilities or programs of a post-secondary educational institution or consortium of the same located in the [C]ommonwealth, or, to the extent that a possibility for such duplication may be found to exist, the center as proposed in the plan may reasonably be characterized as enhancing or supplementing the ability of such an institution or consortium of institutions to conduct such actual or proposed facilities or programs.

Section 6(b)(3) similarly requires the Board to determine that:

> the establishment and operation of the center as proposed in the plan are beyond the financial means of any single postsecondary educational institution or consortium of such institutions located in the [C]ommonwealth.

The Corporation is, therefore, required to confine its activities in the operation of its constituent educational centers to instructional activities which support, and not duplicate or compete with, the facilities and programs of Massachusetts colleges and universities. Further, Section 7(a) provides that

the resources of the centers shall be "made available to participating institutions [of higher education] in a non-discriminatory manner."

Accordingly, while the Corporation has been delegated pursuant to its enabling act a broad discretionary authority to operate its constituent educational centers, the exercise thereof by the Board of Directors is subject to certain limits imposed by statute. The primary statutory purpose of the Corporation is to provide for the expansion within the Commonwealth of sophisticated instructional programs in emerging areas of science and technology. This purpose is, by statutory prescription, to be effectuated by Corporate activities which are consistent with those ascribed to an "educational organization" and an "institution of higher education" by Internal Revenue Code Sections 170(b)(1)(A)(ii) and 3304(f), respectively, which activities are to be undertaken in conjunction with existing institutions of higher education. Further, the Corporation's activities in support of its instructional purpose and function are to be supplemental to and not duplicative of the activities of the colleges and universities of Massachusetts.

3.0 The Massachusetts Microelectronics Center

3.1 Concept

The Massachusetts Microelectronics Center is the first collaborative educational project of the Massachusetts Technology Park Corporation. The Corporation is the Commonwealth's response to a series of distressing developments in engineering higher education. Universities are increasingly frustrated in their attempts to offer sophisticated instruction, attract and develop qualified faculty and support basic and applied research. Capital equipment is expensive to purchase and maintain and rapidly becomes obsolete. Prospective faculty members are all too difficult to attract to the university environment. Research requires both equipment and qualified faculty and, in an era of diminishing federal funding, significant industry support.

Nowhere is the crisis more severe then in the field of semiconductor and microelectronics technologies. The Massachusetts Microelectronics Center, to be funded by the State and private industry, containing the equipment, facilities and technical resources required for advanced educational activities in semiconductor and microelectronics technologies, and accessed on a shared-use basis by a substantial consortium of engineering universities, is the specific response of an unprecedented State-Industry-University partnership. Never before have the State and industry cooperated on a project of this scale. The

consortium of engineering universities participating in the Center project is without parallel in the United States. At stake in the Center project is nothing less than our ability to compete in an age of rapid technology development and intense world-wide technological competition.

3.2 Participating Institutions

The Massachusetts Microelectronics Center supports a unique consortium of public and private engineering universities:

Boston University,
The Massachusetts Institute of Technology,
Merrimack College,
Northeastern University,
Southeastern Massachusetts University,
Tufts University,
The University of Lowell,
The University of Massachusetts at Amherst and
Worcester Polytechnic Institute.

These universities encompass the entire spectrum of technology-based higher education in Massachusetts, a state second to none in the variety and strengths of its institutions of higher education. The consortium has over 12,000 students enrolled in electrical and computer engineering programs and many more undergraduate and graduate students in fields such as

chemistry, physics and materials science who could benefit from an increased exposure to programs in semiconductor and microelectronics technologies. It is estimated that over 2,500 students will participate annually in educational programs supported by the Center. University electrical and computer engineering and computer science departments support a wide variety of research projects in topics such as software engineering, artificial intelligence and hardware design and evaluation.

3.3 Mission

The primary mission of the Massachusetts Microelectronics Center is to provide the engineering universities of the Commonwealth with the capital and technical resources required to enable them to do with distinction in the field of semiconductor and microelectronics technologies what they have traditionally done so well in many other areas: educate engineers for industry, attract and develop qualified faculty and support innovative research activities, and retrain engineers already employed in Massachusetts industry. The primary obstacle to effective university operation in this field is the lack of access to the sophisticated equipment and facilities required for the task. These capital costs of the required equipment and facilities far exceed the resources of any single university or consortium of universities in the State.

The Center provides universities with access to the required equipment and facilities. The Center also provides the participating universities with critical technical assistance, particularly in areas such as facility design and equipment operation. Moreover, the Center accommodates the interests of industry relative to the content of instructional programs, continuing education offerings, short courses, conferences, and symposia for university faculty.

3.4 Structure and Operation

The Center is conceived as an advanced technology facility dedicated to semiconductor and microelectronics technologies. It will have a substantial physical plant, a thirty-six acre campus in Westborough and thirteen satellite facilities located throughout Massachusetts. The Center is financed with an initial capital appropriation from the State in excess of twenty million dollars and matching contributions from private industry, including the largest single contribution ever made to the Commonwealth.

The Center is to have three interrelated elements: (1) a very large scale integration (VLSI) Computer Aided Design (CAD) Network; (2) Distributed Semiconductor Instructional Process Laboratories; and (3) a dedicated, fast turn-around, custom CMOS Integrated Circuit Fabrication Facility. The Center's campus is located near the intersection of the Massachusetts Turnpike and

Route 495. The Westborough campus will house the central continuing education facility of the VLSI-CAD Network and the fabrication facility. Remote facilities of the VLSI-CAD Network and the Semiconductor Instructional Processing Laboratory are located on the campuses of the participating universities.

3.4.1 VLSI-CAD Network

The VLSI-CAD Network consists of a central continuing education facility at the Center in Westborough and seven (7) remote satellite computational laboratories located at participating universities. There will be thirty-six instructional modules in the VLSI-CAD Network, each with a processor or processors having a capacity in excess of 2 million instructions per second, 16 Megabytes (Mb) of memory, 600-800 Mb of disk storage, an operator's console, a 1600/6250 bits per inch tape drive, four high resolution color graphics stations, and four monochrome stations. Printing and plotting capability and communications mechanisms for transferring design layout data to the Center's fabrication facility will be associated with each module.

At this time, the software of the VLSI-CAD Network consists of the University of California (Berkeley) design tools. In the near future proprietary software from VLSI Technologies, Inc will be added. Instruction at the satellite facilities is provided by university faculty. Instruction at the

central facility will be provided by both university faculty and loaned instructors from industry. When completed, the VLSI-CAD Network will be a significant dedicated computational resource for the colleges and universities of Massachusetts.

3.4.2 Distributed Semiconductor Instructional Process Laboratories

The Distributed Semiconductor Instructional Process Laboratories provide students with "hands-on" experiences in semiconductor processing. Students gain insight into the basics of semiconductor process technology and a threshhold appreciation of the complexities of integrated circuit fabrication technology. Students majoring in physics, chemistry, chemical engineering, ceramics, metallurgy and polymers as well electrical and computer engineering students will use this facility.

Each instructional processing laboratory consists of a number of modules located at the campuses of participating universities which are equipped with previous generation fabrication equipment. The laboratories will provide students with the practical educational experience desired by industry and will also serve as the cornerstone for new university research activities in semiconductor processing technology. At the present time, laboratories are under construction at the University of Massachusetts at Amherst, the University of Lowell

(also serving Tufts University and Merrimack College in a consortium) and Northeastern University.

3.4.3 The Integrated Circuit Fabrication Facility

The Integrated Circuit Fabrication Facility will fabricate student designed integrated circuits and return packaged circuits to the students for testing, electrical characterization and completion of the VLSI design educational process initiated through the CAD Network. It will be operated as a CMOS foundry dedicated to fabricating custom student-designed circuits. The distinguishing feature of this foundry will be its ability to furnish finished circuits in less then six weeks. The Fabrication Facility will employ a multi-chip wafer approach for the production of integrated circuits. It will enable the Center to process a significant number of different, custom circuit designs on a single wafer, fabricate the wafers expeditiously in small lots, and return packaged circuits to student designers within a time frame that allows for testing and electrical characterization to be done within the period of a design course.

The opportunity to test and characterize personally designed circuits within a reasonable time after completion of the design process is considered by industry and the participating universities to be a critical component of a comprehensive VLSI design educational program. The detailed

analysis of a fabricated circuit of his or her own design provides the student with a much needed practical exposure to the realities of the fabrication environment. There is no fabrication facility in the United States which efficiently and consistently meets this need. Proprietary foundries are constrained by market forces to place a low priority on student design fabrication. The Center's Fabrication Facility will not be inhibited by such constraints.

With an expanded operation the Fabrication Facility will be able to support an estimated 2,500 students per year in basic and advanced design courses. It is targeted initially to produce approximately 700 full custom student designed circuits each year. Graduate students of the participating universities will be encouraged to use these resources. Future activities may include: (1) supporting collaborative research activities involving industry representatives and university faculty; (2) providing integrated circuit fabrication services for other educational institutions (to the extent consistent with the schedules of the Massachusetts' institutions); (3) providing beta site testing opportunities for industry; (4) engaging in contract research for organizations such as the Semiconductor Research Corporation; and (5) sponsoring short courses, workshops, symposia and conferences in conjunction with industry and the participating universities.

3.5 Implementation Strategies

There are two implementation phases of the Massachusetts Microelectronics Center. The First Phase, currently under way, involves construction of the central campus in Westborough and the full implementation of the remote facilities of the VLSI-CAD Network and the Semiconductor Instructional Process Laboratory element of the Center. The Second Phase of the Center project involves the construction of the dedicated, fast turn-around, custom CMOS integrated circuit fabrication facility. The Second Phase is in the advanced stages of the architectural design process. The Center's attention is presently focused on obtaining commitments from private industry for matching capital contributions. The two phased approach was adopted to enable the participating universities to become thoroughly familiar with their local CAD operations and to allow the Center to devote the substantial effort required to raise funds for the fabrication facility.

3.6 Current Status: Phase I

The Center received State approval to proceed with the First Phase of the Center project in September of 1985. The request to the State was supported by contribution commitments from industry with a value of approximately fourteen million dollars. The State also transfered to the Center a thirty-six acre parcel of the former Lyman School for Boys in Westborough to

serve as the Center's campus and advanced the sum of six and one-half million dollars to cover the costs of renovating the property.

Construction began on the central campus in the Fall of 1985. At the same time, participating universities began to accommodate the Center's remote facilities and participating industries made initial equipment deliveries. A portion of the Westborough campus is presently operational; the First Phase's construction work will be completed by the Fall of 1986.

The construction activities involve the renovation of three buildings for a CAD Center with facilities for ten VLSI design modules and laboratory instructional space, a Classroom Building with ample facilities for a wide range of continuing education activities and an Operational Center for administrative activities. The implementation of the Center's remote facilities is proceeding expeditiously. Each participating university with a satellite VLSI-CAD facility has received at least one design module from the Center and instructional programs are already under way. The full complement of design modules has been scheduled over the next two years to facilitate an efficient integration with existing university facilities and instructional resources. The first Distributed Semiconductor Instructional Process Laboratory will be operational at the University of Massachusetts at Amherst in the Fall of 1986, the second and third will be operational at the University of Lowell and

Northeastern University in the Spring of 1987. Three additional distributed semiconductor laboratories, funds permitting, will be created at participating universities over the next two years.

The Center provides technical assistance to the universities in support of the operation of the CAD facilities. The Center has begun to host comprehensive instructional programs for the faculty of participating universities. The first program for university VLSI design faculty was held in January of 1986, with a follow-up program held in June. A comparable schedule of programs in semiconductor processing is planned after the University of Massachusetts laboratory has become operational. During the Center's First Phase, the Center will provide brokering services for the fabrication of student designed integrated circuits to proprietary foundries.

3.7. Strategy to Achieve Full Operation

It is the Center's objective to have a fully operational three element facility by January of 1988. The implementation of the First Phase of the Center is proceeding on schedule and will be completed by late 1987. The critical path for the Second Phase includes: meeting the private industry contribution match requirement; State approval of the detailed facility and operational plans; and completion of the construction process of the fabrication facility. The Board of Directors of the Center

has adopted the following timetable for the Second Phase of the Center.

Activity	Target
- Submission of Detailed Plan	June 1986
- State Approval	September 1986
- Ground Breaking	September 1986
- Beneficial Occupancy	October 1987
- Fund Raising Completed	December 1987
- Substantial Completion	January 1988

Before the State can approve the Second Detailed Plan, the Center must secure the remainder of the required capital resources. State funds pledged to the project and the matching support received from industry must, in the aggregate, equal the total capital costs of the project. In addition, the total value of the industry capital support must equal or exceed the State's capital contribution.

4.0 The Planning Process: Phase II

4.1 Chronology of Events

This subsection reviews the activities of the Center and the course of the planning process for the Integrated Circuit Fabrication Facility from July 1985, the date of the First Detailed Plan for the Center, to the date of the submission of this Second Detailed Plan. This subsection should be read together with the corresponding subsection of the First Detailed Plan. The First Plan reviewed the Corporation's activities from its inception to July of 1985. That document covered the development of a Definition Statement for the Center, the enactment of a capital outlay appropriation for the Center, the engagement of an executive director, the selection of a site for the Center, the resolution of the Corporation's tax exempt status and the Center's planning process.

At its Fourteenth Meeting on May 29, 1985 the Executive Committee of the Board of Directors of the Massachusetts Technology Park Corporation determined not to include the Integrated Circuit Fabrication Facility in the First Detailed Plan for the Center but to remain committed in principle to the Facility as an essential element of the Center. The Executive Committee determined further to proceed with a Second Detailed Plan including the Fabrication element after further

investigation and upon receipt of sufficient industry contributions.

The Executive Committee's decision to exclude the Integrated Circuit Fabrication Facility from the First Plan for the Center was predicated on two considerations. First, the Integrated Circuit Fabrication Facility is the most complex and expensive element of the Center to construct and operate. As such, more careful concern was appropriate to ensure that the element would serve to further the Center's objectives within reasonable cost constraints. Second, as of May of 1985, industry contributions in support of the Integrated Circuit Fabrication Facility were less substantial than industry contributions for the CAD Network. The perceived reasons for the lack of industry support were detailed in the First Plan. They included the fact that manufacturers of the semiconductor production equipment required for the Integrated Circuit Fabrication Facility were small companies, with less resources to support donations and less familiar with the donations process, located outside of the Commonwealth of Massachusetts. A dramatic downturn in the semiconductor industry had only exacerbated the problem. Accordingly, it was determined that a lengthy and focused contribution solicitation effort was to be required to gain industry financial support for the Integrated Circuit Fabrication Facility.

Immediately after the Fourteenth Meeting of the Executive Committee, the technical staff of the Corporation commenced a comprehensive reexamination of the Integrated Circuit Fabrication Facility. To aid this effort, then Vice Chairperson Jeffrey C. Kalb of Digital Equipment Corporation assigned nine (9) Digital employees to work with the Corporation staff. During the months of June, July, and August of 1985 the Corporation and Digital staffs reexamined the basic Integrated Circuit Fabrication Facility proposal. Equipment needs were reviewed and updated. Operating assumptions were highlighted, scrutinized and reformulated as a series of options for Board review. Operating guidelines were tightened and educational objectives were made more specific.

The need for supporting technical staff was reexamined in light of the foregoing and strict standards were developed for determining the number and classification of the required technical employees. Non-personnel operating costs were scrutinized and crosschecked against the "real world" experience of Digital Equipment Corporation.

During this period, a number of drafts of an operational plan for the Integrated Circuit Fabrication Facility were developed, presented to the Board's Integrated Circuit Fabrication Committee and returned to the staff for review and action. On July 24, 1985, the Integrated Circuit Fabrication Committee granted initial approval of the operating plan for the

Integrated Circuit Fabrication Facility, and directed the staff to prepare a preliminary draft of a complete Second Detailed Plan for presentation to the Board at its next meeting.

The Board of Directors at its Thirteenth Meeting on September 18, 1985 approved this document as a preliminary Second Detailed Plan for the Massachusetts Microelectronics Center. The engineering/architectural firm of Wagner Associates, Inc. of Reading Pennsylvania was directed to begin the design process for the Fabrication Facility. Wagner Associates, Inc. had previously been selected for the project by the Corporation's Designer Selection Panel in a manner consistent with the Commonwealth's Ward Commission statutes.

Immediately and for a period of six months thereafter, the Center was compelled to direct its resources in support of the implementation of the First Detailed Plan. A construction contract was executed with the firm of Granger and Sons, Inc. for site work and the renovation of three buildings on the Lyman School site for the Center in Westborough. Construction began in October of 1985 and is proceeding as of this writing.

Concurrently, the Center initiated negotiations with the State regarding the terms and conditions of a transfer of a portion of the surplus Lyman School site from the State to the Corporation. The issues involved in this transfer were complex. Two State agencies were to be relocated from the property

immediately, with another to follow in the future if certain conditions were met. The dimensions of the property were discussed and a resolution quickly reached. The terms of the transfer to the Center were resolved, including use restrictions imposed upon the Center and the use-rights of State agencies in and on the transferred property. A land disposition agreement was signed by the Center and the State in early February of 1986. As per the requirements of the land transfer legislation, Chapter 405 of the Acts of 1984, the agreement was reviewed by both the Attorney General and the Office of the Inspector General prior to execution. A deed was recorded soon thereafter in favor of the Center with the Worcester District Registry of Deeds.

Also in the Fall of 1985, the Board of Director's committee structure was reconstituted, with an emphasis on more effective Board oversight regarding the affairs of the Center. A new Fabrication Oversight Committee was established to review the implementation of the Center's DSIPL element and the planning for the Fabrication Facility. A substantially expanded Computer Aided Design (CAD) Committee was created. It included representatives from a number of companies in Massachusetts which were not represented on the Board of Directors as well as a number of faculty members from participating universities.

Both the Fabrication Oversight and the CAD Committees have focused their review since the Fall of 1985 on the development of detailed contracts between the Center and the

participating universities. These contracts are to further refine the relationship between the parties to the Center's remote facilities (as that relationship is defined in a preliminary fashion in the Detailed Plan) and incorporate agreements as to the long term activities of those remote facilities. The contract deliberations of the two Committees are on-going as of this writing.

Committees on Budget and Operations, Personnel and Compensation, and Audit were established to ensure that proper budgetary, financial, purchasing and personnel procedures were adopted and implemented. A comprehensive set of Policies and Procedures for the Center were presented to the Executive Committee at its Twentieth Meeting on April 30, 1986. With certain amendments the following Policies and Procedures were adopted: Employee Benefits, Employment Practices, Purchasing Procedures, Relocation Policy, Supplemental Employment/Outside Activities, and Travel and Entertainment Policy.

A Committee on External Relations and Fund Raising, consisting of Dr. Karl Weiss from Northeastern University as Chair and Mr. Robert C. Miller of Data General and Dr. Gerald L. Wilson of MIT, was created. The Committee commenced its work in February of 1986. The Committee found that fund raising was the critical issue surrounding Phase II of the Center and, further, that generating substantial donations of equipment in the semiconductor area would be much more difficult than in the area

of computer aided design. It determined that the Center required a coordinated effort focussed on generating cash contributions from industry. The Committee agreed to explore all alternative possibilities to securing the required support, including: locating donations of acceptable used equipment; determining which, if any, private organizations such as the Semiconductor Research Corporation, would be interested in providing capital funding to the Center; and eliminating mask making from the facility and securing such services from a proprietary organization. It was agreed that the alternative of requesting additional capital funds from the State was the least preferred option.

In April of 1986, the External Relations and Fund Raising Committee initiated a coordinated cash fund raising campaign. Available Center staff were mobilized in support of the effort. Northeastern University agreed to provide a professional fund raiser on a loaned-employee basis. Prospective donors, principally Massachusetts companies, were identified and extensive research undertaken. The Center developed more elaborate brochures and slide presentations and more precise statements of the Center's equipment needs, classified according to priority. The Board of Directors was canvassed to identify all relevant contacts with prospective donors. Working closely with Governor Dukakis, the Committee attempted to ensure that prospective donors were aware of the Governor's support of the Center project. In addition, the Center's executive director

continued to solicit contributions of semiconductor fabrication equipment from industry.

The External Relations and Fund Raising Committee determined that it was feasible to generate the required industry contributions in support of the Fabrication Facility. The Committee recommended that the Center proceed with the submission of the Second Detailed Plan. A draft Plan was presented to the Executive Committee at its Twentieth Meeting on April 30, 1986. At the Twenty-first Meeting of the Executive Committee on May 28, 1986 the Executive Committee directed the staff to clearly indicate what portion of the proposal for the Fabrication Facility was absolutely necessary for the Facility to serve its intended function over the five year (Fiscal Years 1987-91) period covered by the Plan. The staff was instructed to prepare a proposal for a baseline Fabrication Facility which requested State approval for just that necessary portion. The staff was further instructed to detail proposals to augment the baseline Facility in future years if funds were made available for this purpose. The Board of Directors of the Center approved the baseline Fabrication facility proposal at its Sixteenth Meeting on June 18, 1986. The Board made three of the factual findings required by the Corporation's enabling act and delegated to the Executive Committee the authority to make the final finding regarding contribution commitments. The Plan was submitted to the State as a preliminary document on that date. The Executive Committee made the fourth finding of fact on August 27, 1986.

4.2 Statutory Requirements

The statutory requirements associated with the Detailed Plan for the Center are set forth in Section 6 of Chapter 40J of the Massachusetts General Laws. A preliminary review of these requirements is appropriate to establish a frame of reference for this planning document. Section 6 of Chapter 40J provides that the Corporation shall establish a center only after formulation of a "detailed plan" for such a center, "provided that the plan shall be supported by independently verifiable information." Section 6(a) proceeds to prescribe the elements of a center's detailed plan. Section 6(b) requires the Corporation's Board of Directors to make certain "findings of fact" regarding a center as proposed in a plan; and Section 6(c) directs the Board to submit a plan for a center to certain State officials.

In summary, Section 6(a) provides that a detailed plan must include: an educational program (entitled herein, "Equipment and Operation"), a facilities program for a center (entitled herein, "Real Property"), projections of the capital and operating costs associated with a center, including a projected allocation of these costs among the State, industry, and university parties to a center partnership (entitled herein, "Budgetary Materials"), and an analysis of the benefits expected to inure to the Commonwealth from the operation of a center (entitled herein, "Benefits of the Center").

The educational program requirements are established by Sections 6(a)(1) and 6(a)(5) of Chapter 40J. Section 6(a)(5) prescribes an educational program for a center by providing that a detailed plan must include:

> a description of the proposed activities of the center, including the proposed utilization thereof by participating businesses and participating institutions.

Section 6(a)(1) establishes the facilities program requirement. It provides that a detailed plan must include:

> a detailed description of the proposed center, including an analysis of all lands, structures, facilities, machinery, and equipment reasonably necessary for the successful operation thereof. . .

The Budgetary Materials requirements are established by Sections 6(a)(1), (2), and (6) of Chapter 40J. Section 6(a)(1) calls for a capital cost budget in support of the creation of a center, which must include certain State supported costs related thereto. This section requires that a plan for a center include:

> a statement of the proposed project costs reasonably associated with establishing such a center, with a detailed breakdown of such project costs, including an estimate of the cost to the [C]ommonwealth of the debt

> service on any bonds or notes issued or to be issued in support of such a center.

Section 6(a)(2) mandates a five year capital and operating budget for a center. It provides that a center's plan must include:

> a statement of the proposed annual start-up expenses, project costs, and current expenses of the center for the first five years of its existence, including a detailed breakdown of such costs and expenses.

Section 6(a)(2) and 6(a)(3) require that a center's plan include projected allocations of its five year capital and operating expenses among the State, industry, and university parties to a center partnership. Section 6(2)(2) requires

> a reasonable projection of that portion of said [capital and operating costs] and expenses which the corporation expects to meet through assistance provided by participating businesses, rates, rents, fees, and charges imposed upon users and support from any other sources. . .

And Section 6(a)(3) requires:

> a description of the assistance to be provided to the corporation in support of the center by participating

> businesses and participating institutions, with evidence of such assistance and the terms and conditions thereof, if any;

Finally, Section 6(a)(6) directs that a center's funding requirements be expressed in formal appropriation requests to the State. It provides that a center's plan must include:

> a proposal for a capital outlay appropriation from the [C]ommonwealth in support of the establishment of the center and such annual maintenance appropriations as may reasonably be required for the successful operation of the center.

The benefit analysis requirements of a detailed plan for a center are established by Section 6(a)(4) of Chapter 40J. This section specifically recites that a plan must include:

> a description of the public benefits to be engendered by the center, including particularly an analysis of increased and enhanced employment and educational opportunities.

Section 5(b) of Chapter 40J requires that the Board of Directors of the Corporation, after formulating its detailed plan for a center, must make certain "findings of fact" with regard to the center as proposed in the plan for the five year period

encompassed by the plan: that it is consistent with the Corporation's statutory mission to support instructional programs in emerging areas of science and technology; that it does not propose to duplicate the existing resources of traditional institutions of higher education; that it is beyond the financial means of traditional institutions of higher education to support; and that industry and universities have agreed to provide certain support for a center's creation and operation. Section 6(b)(4), which establishes the industry match requirements, is of particular interest. It provides that the Board must find that:

> The corporation has received appropriate commitments from participating businesses and participating institutions to support the center and to maintain a continuing effort to support the center; provided, that the commitments from participating businesses for project costs and start-up expenses shall be for support which, in the aggregate, is equivalent in value to the amount of the proposed disbursement from the center fund and which support includes provision of the equipment and machinery necessary and appropriate to establish the center as provided in the plan; provided, further, that the commitments from participating businesses to maintain a continuing effort to support the center shall include commitments to provide the equipment and machinery necessary and appropriate to ensure that the center is maintained at a level consistent with

developing technology; provided, further, that the commitments from both participating businesses and participating institutions to maintain a continuing effort to support the center shall include commitments to provide qualified individuals from among the employees thereof to serve from time-to-time as instructors at the center; provided further, that the provision of equipment, machinery, instructors, and support for any other kind by participating businesses and participating institutions shall be at no charge to the corporation; and provided further, that the value of said equipment, machinery, instructors, and other support shall be determined by executive director of the corporation.

Finally, Section 6(c) requires the Board of Directors of the Corporation to submit the foregoing detailed plan and findings of fact regarding a center to the Governor, the President of the Senate, the Speaker of the House of Representatives, the Chairman of the Senate Committee on Ways and Means and the Chairman of the House Committee on Ways and Means. The fifth paragraph of Section 5 of Chapter 40J provides that "no monies shall be credited to the center fund in support of a particular center" unless and until the plan and findings required pursuant to Section 6 of Chapter 40J "have been received and approved in writing" by the House and Senate Committee on Ways and Means.

5.0 The Integrated Circuit Fabrication Facility

5.1 Introduction

In a manner consistent with the legislative requirements associated with the Detailed Plan for the Center, this section is organized around four general subsections: Equipment and Operation, Real Property, Budgetary Materials and a Benefit Analysis, in that order.

5.1.1 Equipment and Operation

The Equipment and Operation subsection describes the Integrated Circuit Fabrication Facility in detail. It proposes a baseline Facility with the capacity to fabricate a limited number of student-designed circuits ranging from full custom to gate array designs in a fast turn fashion. Proposals to augment the baseline Facility are also reviewed as options for consideration in future years. The baseline Facility materials contain: an introduction with a statement of the element's educational objectives; a description of the operational guidelines of the baseline Facility; a review of the Facility's process; a review of the wafer fabrication and test/assembly components of the Facility; a description of the equipment required for the Facility; a review of the manpower requirements of the Facility; and a proposed operational budget for the Facility. This subsection is intended to provide a statement of the educational

objectives of the Fabrication Facility. It also contains information sufficient to support the facilities program contained in the Real Property subsection, the information contained in the Budgetary Materials subsection and the representations made in the Public Benefit Analysis subsection.

5.1.2 Real Property

The Real Property subsection discusses the new Semiconductor Building proposed for the Center in the form of a detailed facilities program. Included as integral elements are capital budgets for the design and construction activities proposed for the site and an incremental staffing and operating budget for site administration costs associated with the Semiconductor Building. The Real Property subsection further summarizes the manner in which the Semiconductor Building could support additional operations of the Center in the future. Appendices to the Real Property division are as noted and are included at the end of the division.

5.1.3 Budgetary Materials

The Budgetary Materials subsection separately states the budgetary information referenced in the Descriptive materials subsection in a project cost (capital cost) budget, a five year operating budget and a proposal for State appropriations in support of the Center. All budgetary figures are specifically

represented as supporting the minimum educational objectives and activities of the Center and are presented as Fiscal Year 1986 dollars with a first fully operation Fiscal Year of 1989.

5.1.4 Benefits of the Center

The public benefits analysis subsection recites briefly those benefits which are expected to inure to the parties to the Center partnership and to the Commonwealth as a whole from the proposed public investment in the creation and operation of the additional elements of the Center. Finally, exhibits referenced in one of the foregoing subsections are found at the conclusion to that division.

INDEX: SECTION 5.2

5.2.1 Introduction

This Plan proposes to augment the Center described in the First Detailed Plan by the addition of an Integrated Circuit Fabrication Facility. The Fabrication Facility will be the most expensive element of the Center to design, construct and operate and will be its most technically complex element. It is intended primarily to fabricate integrated circuits designed by students through the resources of the VLSI-CAD Network. This Plan proposes a "baseline" Fabrication Facility. The baseline Facility is targeted to a threshhold level of operation with concomitant equipment, staffing and budgetary plans but with a structure designed to accommodate increased levels of operation and the demands of developing technology. The structural capacity of the baseline Facility will enable the Center to expand the operation level in future years to meet anticipated university demand for fabrication services through the addition of equipment, manpower and operating budgets. No additional buildings will be required.

The baseline Facility proposed in this Plan has two major components: wafer fabrication and test and assembly. Sections 5.2.2 through 5.2.8 review the operational guidelines and process of the baseline Facility, the wafer fabrication and test and assembly components, the equipment and manpower plans and the operating budget of the baseline facility. Section 5.2.9 reviews plans to expand the fabrication capacity of the baseline

Facility in future years. Specifically, Section 5.2.9 details proposals to incorporate an internal mask making component to the Facility and to add certain items of equipment, staffing and operating funds necessary to increase fabrication services in a fast-turn fashion.

The primary objective of the Integrated Circuit Fabrication Facility is to fabricate an established number and product mix of student designs within the design course cycle, (referred to as a "fast-turn cycle time") and to return the fabricated circuits to the student in a form amenable to testing and characterization. At the present time, very few of the colleges and universities of Massachusetts have the independent computational capabilities to support instructional programs in VLSI design. Even universities which have a computational capability through the Center or otherwise which is sufficient to support theoretical VLSI design courses lack the facilities to provide the student with a work product of their design courses. The Integrated Circuit Fabrication Facility will consist of the capital facilities, scientific equipment and machinery and technical staff required for the fabrication of integrated circuits. It will provide VLSI students with a legitimate real time laboratory experience.

The decision to incorporate a proposal for an Integrated Circuit Fabrication Facility in the plan for the Center was made only after a lengthy review by the Board of Directors of the

importance of a laboratory experience to VLSI design programs and a detailed review of alternatives to providing this experience through an in-house fabrication facility at the Center. Because a fabrication facility is so difficult and expensive to create and operate, the standard employed by the Board was that any reasonable alternative which supported this practical component within the required time and characterization parameters would be preferable. Unfortunately, it was found that no reasonable long-term alternative existed.

The technical expertise and financial resources required to support a captive fabrication facility were found to greatly exceed the individual or collective resources of Massachusetts colleges and universities. The alternative of brokering student designs directly through a proprietary integrated circuit foundry or indirectly through a separate brokering institution was found to be unsatisfactory on a long term basis. Current university experience is that it takes between ten and fourteen weeks from the time a design is shipped to the time it returns to the student for testing and characterization. The integrated circuit is returned to the student so long after its design that its practical value is limited. The Board was therefore compelled to include an Integrated Circuit Fabrication Facility as an essential element of the Center.

5.2.2 Operational Guidelines

The plan for the construction and operation of the Integrated Circuit Fabrication Facility has proceeded pursuant to a number of operational guidelines. The operational guidelines are predicated upon one general standard: that the Integrated Circuit Fabrication Facility should support the minimum, practical component which is necessary for a comprehensive VLSI design curriculum and which is consistent with reasonable expectations of capital and operating support from the State, industry and participating universities. The operational guidelines concern: the type of technology to be employed; the minimum feature size (geometry) to be incorporated into facility and operational plans; the breadth of student design flexibility to be supported by the facility; and the quantity of designs and wafers to be processed. These operational guidelines are reviewed below.

5.2.2.1 Type of Technology

The Integrated Circuit Fabrication Facility will employ a type of processing technology known as Complimentary Metal Oxide Semiconductor (CMOS). The CMOS process is considered to be the most universally applicable technology available to support the fabrication of VLSI designs. A CMOS facility will be the most flexible. It would have the capability of fabricating numerous other MOS processes, and as certain bipolar processes.

5.2.2.2 Minimum Feature Size

The choice of a line-width geometry for the Fabrication Facility raises issues regarding the activities to be supported by the Facility and has critical implications for the scientific equipment and machinery and capital facilities required to support those activities. The capital facilities have been designed to support the fabrication of minimum feature sizes required to serve the Facility's basic purpose in late 1987. Anticipating future developments, the capital facilities will support the fabrication of integrated circuits with less than one micron line-widths to preclude early obsolescence of the Facility. However, the level of activity proposed for the actual operation of the Fabrication Facility at its inception will be substantially less than the capability of the capital facility. Design ground rules will be limited initially to a 2 micron feature size. As process technology matures and as designs become more sophisticated, the minimum feature size restriction will be capable of being extended below the 1.0 micron level.

5.2.2.3 Design Flexibility to be Supported

After detailed discussions among the industry and university representatives on the Board of Directors, it was determined that the level of student design flexibility to be supported by the Fabrication Facility is to be consistent with

the Mead-Conway approach to VLSI design currently employed at major universities to support VLSI design theory. The function of the Center is to provide the missing practical component to this instructional approach. The Facility should be capable of providing services for a complete range of designs, from gate array to full custom. This operational guideline has profound capital facility and equipment implications as the Facility must have all the capabilities associated with a proprietary integrated circuit foundry.

5.2.2.4 Quantity of Designs

As stated earlier, the Fabrication Facility is designed primarily to fabricate the integrated circuits designed by university students through the resources of the VLSI CAD Network. Based on current projections as to the number of participating students, the Board has adopted a baseline level of approximately 700 full custom and 1000 gate array designs per year. The baseline target provides the Center with the lead time necessary to make this technically complex facility operational. It is anticipated that student demand could increase in future years to approach 2,500 designs/year.

Since only a small number of complete circuits must be fabricated for each design, numerous designs will be fabricated on a common mask set and a common lot of wafers. If this approach were not employed, the number of photomasks and

processed wafers required would be prohibitive. In order to determine the optimum number of unique designs that can be effectively fabricated on a given mask set several factors must be considered:

1. Wafer size
2. Die size
3. Process yields
4. Wafer lot size
5. Die/design/wafer

The rationale used to make these determinations will be discussed for each factor.

5.2.2.4.1 Wafer Size

VLSI Technology, Inc., the firm that will supply the CAD tools and could supply the process technology, will employ 125 mm wafers in the 1987-88 time frame. In order to be compatible the Center foundry must be based on 125 mm wafers.

5.2.2.4.2 Die Size

Die must be sufficiently large to accommodate full custom VLSI designs as well as gate arrays. Although some current VLSI designs, such as 32-bit microprocessors, can exceed 0.300" per side, this level of design complexity will not

represent the majority of designs received at the Center. Additionally, although gate arrays range in die size from 0.140" per side to 0.450" per side, the bulk of the designs anticipated should not be at the extreme high end of the range. A die size approximately 0.200" per side should meet most design needs.

Recognizing that it will be necessary to fabricate some number of aggressively sized designs, the bulk of the designs, especially those planned for fast-turn fabrication, should be compatible with a single, standard die size. The standard die size will provide significant cost savings and cycle time efficiencies in all processing areas of the Center. A target die size of approximately 0.200" per side with design rules for assembly compatibility (detailed in the Assembly section) results in a die size of 0.192" X 0.192". This die size will provide about 450 gross die on a 125 mm wafer, and is ideally sized for use in a 68 pin package. A standard, inexpensive 68 pin lead-less chip carrier will be employed for all fast-turn designs. It should be emphasized that although other die sizes and package configurations can be employed, the 0.192" per side die and the 68 pin lead-less carrier will be the fast-turn standard.

5.2.2.4.3 Process Yields

The following yields were established based primarily upon accepted industry standards for VLSI designs and CMOS

processing, but with some accommodation for the prototype nature of the Center's activity.

- Wafer Fab 80%
- Functional Probe. . . 20%
- Die Screen. 60%
- Assembly Yield. . . . 90%

The 80% wafer fab yield means that, on the average, 80% of the wafers that start the wafer fab process will successfully complete that process, and be suitable for further processing.

The 20% functional probe yield is an assumed number based upon conservative, historical VLSI yield models. Actual functional testing will not be performed at the Center, but at the university by the designer. Since the functional die (20% average) in the individual population of each design are therefore unidentifiable, an electrical test for continuity and excess leakage currents will be performed to screen the population for grossly defective die. It is assumed that this screening will remove 40% of the grossly defective die (60% screen yield). The percentage of potentially functional die in each population should approach an average of 33% thereby increasing the probability of choosing "good" die to process through assembly and packaging. Finally, it is expected that only 90% of the die starting the assembly process will successfully complete it.

5.2.2.4.4 Wafer Lot Size

Due to the requirement for fast-turn fabrication, it is desirable to minimize the work-in-proces inventory in wafer fabrication. Equally important is small lot size, so that a given group of wafers can quickly pass through a given unit process. There is, of course, a lower limit since as the number of wafers per lot decreases, the impact of a single wafer loss increases. In actual practice, lot sizes exceeding 10 wafers begin to add appreciable cycle time to the wafer fab process.

5.2.2.4.5 Die/Design/Wafer

In order to perform even the most rudimentary electrical characterizations, the designer should receive about 5 functional units. In order to approach this outcome, significantly more die than 5 must be packaged. However, due to capacity and cost limitations in the assembly area, the maximum number of units to be packaged per design has been set at 25.

Taking these factors into account, and incorporating the previously defined process yields, the problem of determining the optimum number of designs that should be combined on a given set was addressed by D. Priore of Digital Equipment Corporation's Technology Group. His detailed analysis is included in Exhibit 5.2.2. The data shows that, at one extreme, placing four (4) die

per design on a mask set (over 100 designs per 125 mm wafer using a 0.192" die size) results in failure to achieve the goal of five (5) good units for 33% of the designs. As the number of die per design per mask set increases, the probability that less than five (5) good units will be fabricated ranges from 9.5% to 9.1%. The data also shows that the probability of obtaining at least one (1) functional die exceeds 99.79% in each case, statistically assuring that each designer would receive at least one (1) functional unit. Based on this data, the goal of forty (40) designs per 125 mm wafer has been targeted for planning purposes.

It should be recognized that if the 0.192" square die fails to accommodate the bulk of fast-turn designs, the standard die size will need to be increased. The net effect of any such increase in die size will be a proportionate reduction in the number of individual designs that can be combined on a given mask set. There are two other factors which will impact the actual number of designs that can be combined on one mask set. First, the use of standard test patterns for process parameter and defect density measurements will occupy positions normally used for device designs. Second, there are several geometric considerations regarding die placement that must be reconciled with the mask making and inspection process. The Board is confident that the foregoing issues will be resolved favorably; accordingly, this Plan has been predicated upon a 40 designs per make set target.

5.2.3 Process Overview

Student design data from the VLSI-CAD Network element of the Center will be forwarded from the participating university remote CAD sites to the Center. The Center will coordinate and schedule the process of fabricating electron beam ("E-beam") photomasks by an external mask making facility. E-beam mask making has been chosen since it can achieve much higher throughput rates than optical mask making and is less expensive to operate. E-beam mask making eliminates the need for both pattern generation and reticles. Layout data is written directly onto the photosensitive mask surface. At the quantity of design level proposed for the baseline Fabrication Facility, it is cost-effective to employ a proprietary mask making facility to secure the required photomasks. If the Center is to increase the fabrication capacity of the Facility substantially in future years, an in-house mask making capacity will be required in future years as a practical matter. (See Section 5.2.9).

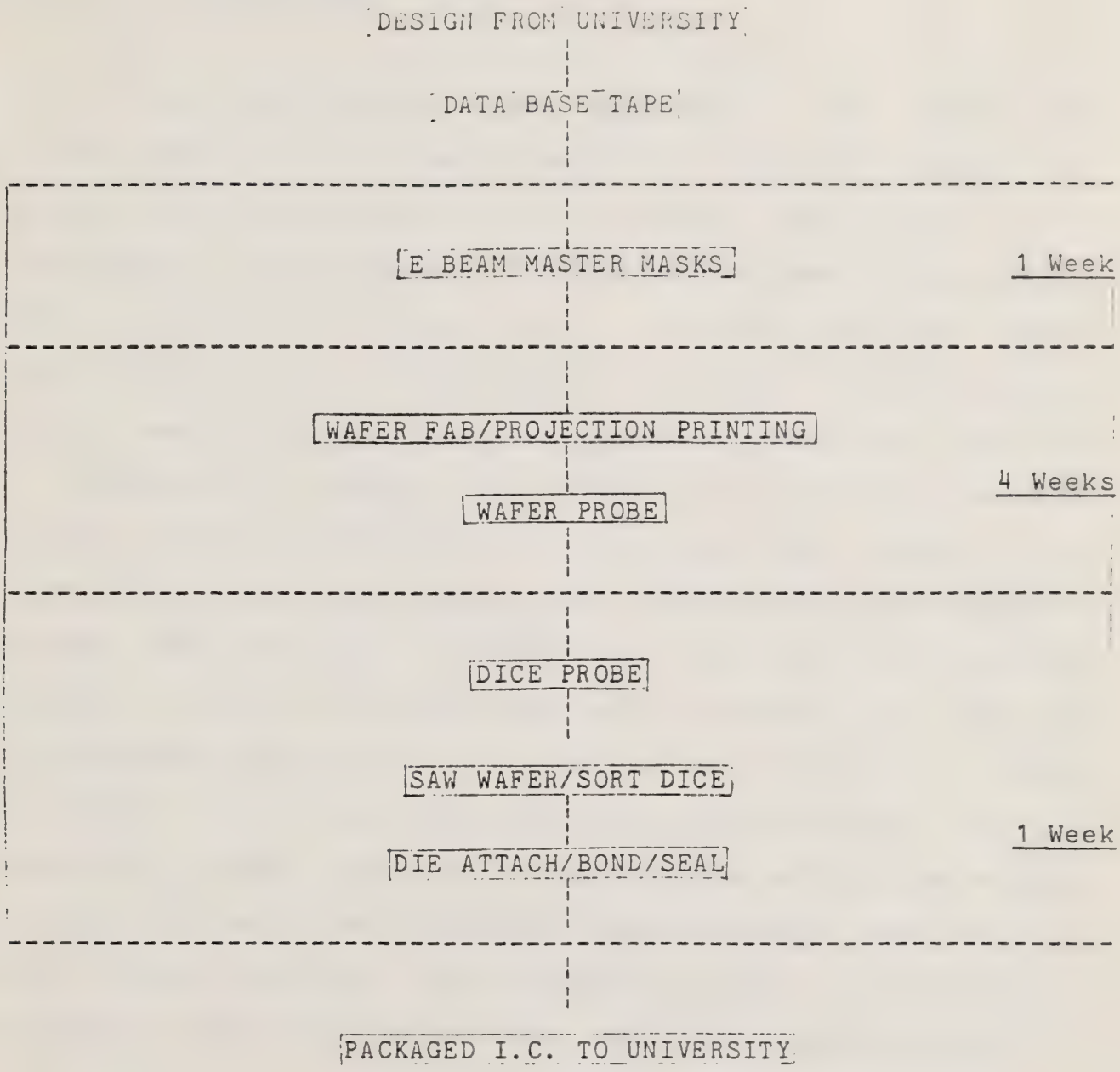
To accommodate the requirement for fabricating small numbers of circuits but a large number of designs, numerous designs will be fabricated on the same wafer (multi-project wafer approach). This will substantially reduce the number of wafers as well as the number of photomasks to be processed. As reported earlier, the Wafer Fab Facility will employ a fixed CMOS process technology, capable of both single and dual layer metalization. The wafer fab area will be staffed and equipped to provide an

average four week cycle time for designs adhering to fast-turn guidelines.

The assembly area will be capable of packaging the output of the wafer fab area on a weekly basis. All fast-turn designs will be fabricated on one standard die size, using a standard pin-out configuration, and a standard package. These restrictions will not only streamline the assembly operation, but will also enhance operating efficiencies in both mask making and wafer fabrication.

The two major segments of the facility, Wafer Fabrication, and Test and Assembly, are detailed in the following sections. The overall process for fast-turn fabrication is depicted in Figure 5.2.1, accompanied by the target cycle times in each key area.

FIG. 5.2.1 PROCESS OVERVIEW



5.2.4 Wafer Fabrication

5.2.4.1 Process Time

The exact CMOS process employed in the Wafer Fab Facility remains to be determined. For planning purposes, a 12 mask level CMOS flow typical of those used by many I.C. manufacturers was provided by the Digital Equipment Corporation, and is included in Exhibit 5.2.1. Indicated operation times shown in Exhibit 5.2.1 are actual in-process times employing current semiconductor processing equipment. The total time of all operations in Exhibit 5.2.1 equals 98.3 hours and is the minimum theoretical time for a 12 level process. Figure 5.2.2 depicts the number and nature of key operations in this typical 12 level CMOS process. It should be noted that the process depicted in Figure 5.2.2 and detailed in Exhibit 5.2.1 can be utilized with either one or two levels of metalization. In order to minimize cycle time, all fast-turn custom designs will be restricted to only one layer of metalization while gate arrays will utilize two. The theoretical process cycle time for the CMOS process with only one metalization level is 86.8 hours, compared to 98.3 hours for the dual layer metalization process.

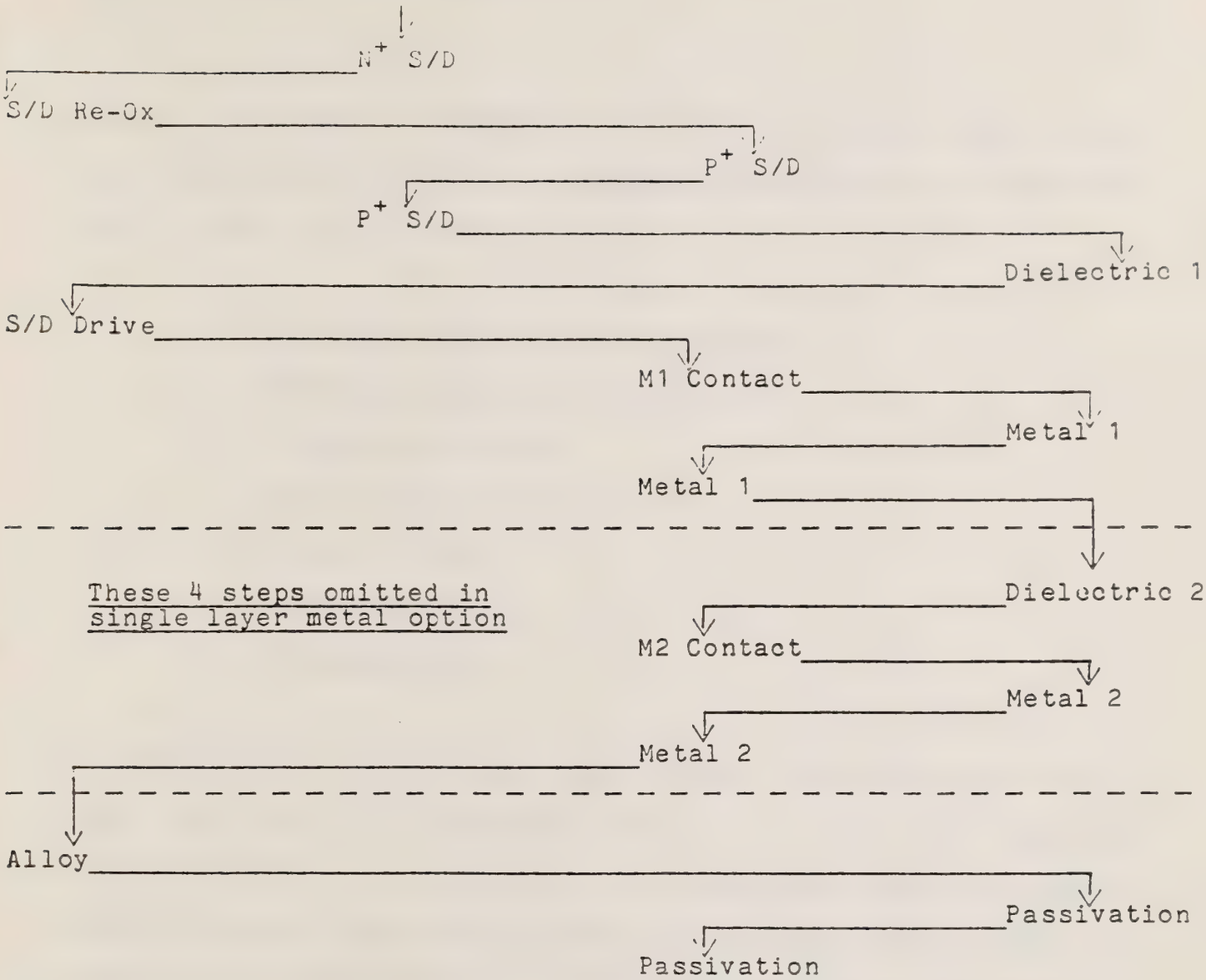
FIGURE 5.2.2

12 LEVEL CMOS PROCESS

THERMAL	IMPLANT	PHOTORESIST	DEPOSITION
Well masking Ox			
		N Well	
	N Well		
Well Drive			
Initial Ox			
			Nitride
		Nitride	
	N Channel Field		
		P Channel Field	
	P Channel Field		
Field Ox			
1st Gate Ox			
	V_T Adjust		
		N Channel V_T	
	V_{TN} Adjust		
2nd Gate Ox			
			Poly
Poly Doping			
		Poly	
		N^+ S/D	

(CONTIUNED)

FIGURE 5.2.2 (Cont'd.)



5.2.4.2 Wafer Requirements

In order to establish a wafer throughput requirement, the following operational guidelines, developed in the previous section, will be utilized:

- 700 full custom designs/semester
- 1000 gate array designs/semester
- 4 week cycle time
- 0.192"/side die size
- 125 mm wafers
- 40 designs/wafer
- 10 wafers/lot

To smooth the work load and still retain fast-turn cycle time, each week for four consecutive weeks 1/4 of the lots required will be started. In week 5 of the 8 week time period the first group of wafer lots would be completed (4 week cycle time). In week 8 of the time period, the final group of wafer lots would be completed. This system will require member universities to submit designs for fast-turn processing according to a rigid, pre-determined time table.

5.2.4.3 Wafer Throughput

To satisfy the Center's fast turn requirement, wafer throughput must be optimized during certain peak periods. It is important to recognize that the fabrication line does not start from a zero inventory when these peak periods arise. The line will always carry a work-in-process inventory essential to maintaining statistical process control and insuring a "working" process when new designs are started. It is anticipated that about 50 wafers per week will be started even during off-peak times and that the cycle time during this period would also average four weeks, as required during fast-turn processing. A "run rate" of 50 wafer starts per week represents the minimum run rate of the Facility and will support the baseline operation of the Facility. As the peak loading period begins, fast-turn lots will be started in place of the process control lots.

The maximum work-in-process inventory during peak load periods can be approximated by summing four weeks of wafer starts while accounting for wafer fab yield losses. At 50 wafer starts per week with an 80% fab yield the work-in-process peak would build to about 190 wafers, distributed among 20 lots.

A partial summary of this data is found in Table 5.2.1

TABLE 5.2.1

PARTIAL THROUGHPUT SUMMARY

FOR

FAST TURN PERIODS

Wafer starts per week	50
Wafer outs per week	40
Cycle time plan (weeks)	4
Work in process (wafers)	190

The 190 wafers will be distributed among 32 major process steps. Since the required cycle time is 4 weeks (20 days), all 190 wafers must theoretically pass through an average of 1.6 major process steps each day (32/20). In reality, this does not occur since process lengths vary and queuing occurs at common equipment interfaces. However, since all these wafer movements must occur within the planning cycle time, the work-in-process model provides valuable planning data.

It is also necessary to consider wafer throughput in the context of wafer lot size; that is, the number of identical wafers being processed as a group. The 190 wafer inventory divided among 20 lots translates into an average of 0.6 lots at each process step (20 lots/32 major process steps) of the 10 PR level process. Similarly, since all wafers must theoretically move through 1.6 process steps each day, moving the 190 wafer inventory 1.6 times each day is equivalent to about 300 wafer movements each day (1.6 x 190). Adding this data to our partial summary table, results in Table 5.2.2.

TABLE 5.2.2

THROUGHPUT SUMMARY

FOR

FAST TURN PERIODS

Wafer starts per week	50
Wafer outs per week	40
Cycle time plan (weeks)	4
Work in process (wafers.	190
Major process steps	32
Process steps required per day. . . .	.1.6
Wafer movements required per day. . .	300
Wafer movements per process step per day.	9.4
Lots per process step (Average)	0.6

Once wafer movement requirements are defined it is possible to establish the throughput capacity required in each of the key process areas of photolithography (particularly in wafer alignment), diffusion, ion implantation, and film deposition. The primary bottleneck in a wafer fabrication facility is the photolithography area, more specifically, the alignment/exposure operation. Despite the extravagant claims of equipment vendors, a realistic throughput limit for a projection alignment system is about 40 wafers per hour. Assuming one shift of operation, one aligner can therefore turn 1,275 alignments per week (40 alignments/hr. x 7.5 hrs/day x 5 days/wk x 0.85). However, this data is based on normal production conditions. The MMC foundry will be processing about 12 small lots through the alignment area each day, requiring 12 mask changes. Each mask change requires at least 10 minutes, thereby consuming about 2.0 hours of alignment time each day, and must be accounted for in any capacity calculations. This represents a weekly loss of 400 alignments (2.0 x 5 x 40).

In terms of daily wafer alignment capacity requirements, the 12 mask level process dictates that an average of 104 wafers must be aligned each day. (9.4 movement/day/step x 10 mask steps x 1.1). The 1.1 factor accounts for anticipated rework in photolithography. In reality, the even distribution of work-in-process at all process steps will rarely occur on a daily basis. Nevertheless the same number of alignments must be accomplished at some time during the process sequence. It is

therefore valid to plan on a weekly alignment requirement of about 520 alignments (104 x 5). To this must be added the 400 "lost" alignments, totaling 920 per/week.

The diffusion area will not be taxed in terms of wafer quantities to be processed. Dedicated furnace tubes will preclude this area from becoming a limit to fast turn throughput. The logistics of the ion implantation area are complicated by the need to process numerous small lots of wafers through boron, phosphorous and arsenic implantation each day. It will be necessary to shut the implanter down while switching sources at least twice each day, a severe throughput limitation. It requires about 45 minutes to purge and qualify the system between source changes. As a result, the ion implant area will probably be faced with periodic extensive back shift overtime activity. The mix of dedicated equipment available in the thin film/CVD area will permit smoother movement of materials than in ion implantation, but will suffer the same queuing problems at certain process steps.

Table 5.2.3 is a summary of the daily wafer/lot movement requirements for each process area.

TABLE 5.2.3

DAILY WAFER/LOT MOVEMENT REQUIREMENTS

Photoresist*. . .	103/12
Diffusion	92/10
Ion Implantation	66/8
Thin Film/CVD . .	55/6

*Includes 10% rework

5.2.4.4 Cycle Time

Referencing Exhibit 5.2.1, the minimum process cycle time attainable in a 12 mask level CMOS process is about 100 hours (98.3). With only one metal level (10 level process) the time is reduced to 87 hours. It must be recognized that these times are exclusive of queuing, downtime losses, reworks, or other delays. They represent the actual time required to move one small lot of wafers through the fabrication area.

As noted earlier the target cycle time for wafer fabrication is 4 weeks. On a one shift basis, then, over 2 weeks (87 hours) of the total 4 weeks is consumed by actual in-process time. Calculations based on equipment, throughput capacity and cycle time result in an average lot queue time of about 24 hours for the ten level fast-turn process. Mask changes noted earlier will add significant queue time. Employing a typical equipment downtime of 20% consumes 22 more hours. Another cycle time delay that must be considered is the extensive source switching required of the one ion implanter, which will further impact cycle time.

Adding a 10% process downtime results in the total cycle time depicted in Table 5.2.4.

TABLE 5.2.4

CYCLE TIME

Theoretical cycle time (Hrs.)	87
Queuing time (Hrs.)	24
20% Equipment downtime (Hrs.)	22
Mask changing (Hrs.)	4
Ion Implant changes (Hrs.)	17
10% Process downtime (Hrs.)	11
Total (Hrs.)	165
Target (Hrs.)	160
to target (Hours.)	-5

5.2.4.5 Product Mix

Thus far, this plan has concentrated on the requirements for fabricating full custom VLSI designs, i.e., those designs that utilize unique photomasks for each patterning level in the process. Attention will now be shifted to another category of VLSI designs called the Gate Array.

The Gate Array is a semicustom integrated circuit that is produced from a standard wafer containing unconnected gates or components; these devices are connected ("personalized") during the final stages of processing to produce the desired circuit. The use of a standard wafer up to the personalization levels means that a common supply of previously fabricated wafers can be customized through the use of only three (3) unique photomasks for each design, rather than the nine (9) to twelve (12) required in a full custom circuit.

The standard wafers can be fabricated well in advance of the time they would be utilized, and held in inventory just prior to the customizing levels. Since about 75% of the wafer processing is completed in advance, the cycle time to complete fabrication of the personalized wafers would be drastically reduced. Even though gate array fabrication requires the use of dual layer metalization, thus increasing theoretical process time from 87 to 98 hours, most of the process time would have occurred in off-peak periods. The theoretical process time for completing

a gate array from stockpiled wafers is 22.5 hours compared with 86.8 hours of process time for a single metal level, full-custom design. As gate arrays represent a significant portion of the VLSI designs to be fabricated in the baseline Facility, the pressure of peak-load periods is reduced in making area and the wafer fab area. Operational costs are also reduced significantly.

5.2.5 Test/Assembly

5.2.5.1 Wafer Probe

All wafers will contain a standard group of test vehicles which will permit DC parametric testing as well as defect density measurements. Probing of these test patterns will provide quantitative evidence that their host wafers were subjected to processing conditions sufficient to produce active components within design specification limits. This data will be used to determine which wafers should be forwarded to the assembly process, and to develop a statistical data base for process control purposes. If feasible, the probing of the DC parametrics may be combined with a rudimentary "go/no-go" test of the VLSI designs. This test will merely screen chips for opens, shorts, and excess leakage currents. No functional testing will be attempted. This screening should however, significantly increase the number of potentially functional die in the

population of chips that will be processed through the assembly and packaging processes.

5.2.5.2 Assembly

The assembly process flow is depicted in Figure 5.2.3. It should be noted that in the interest of reduced cycle time, process simplicity, and minimized capital investment, wafers will not be backlapped prior to assembly. Nor will the wafers be gold-backed since epoxy die attach will be employed. Wafers will be tape mounted and attached to metal film frame carriers. They will then be sawed on tape using a full depth cut. After a gross inspection 25 chips of each design will be transferred to matrix waffle packs for subsequent assembly. Sorting by device at this point in the process is under consideration. However, it may be more efficient to process all chips in one lot. This decision has little impact for planning purposes and will be deferred.

The next step in the sequence is epoxy die attach. This of course, will preclude any design dependence on back side electrical contact. Epoxy curing will be by nitrogen purged Blue M batch ovens at approximately 150 degrees centigrade. Wire bond will be accomplished by gold ball thermosonic bonding. Gold ball bonding has been chosen since it is faster and it is a more mature technology than aluminum wire bonding. Only one bonding program will be required since only one bond pad layout will be

layout will be utilized. To further simplify operations, all pads will be bonded whether or not they are used on the chip.

The pre-seal visual inspection will require stereo-zoom microscopes. This may ultimately be the design sorting inspection point. Any missing or defective bonds can also be repaired at this point using a manual bonder. The sealing operation is intended only for mechanical protection. Ceramic lids with pre-applied epoxy will be used for lidding. Curing will be performed in the same ovens used for die attach cure. The marking system will be an ink jet system with an air or UV cure. After marking, packaged units will be shipped in conductive plastic sleeves.

FIGURE 5.2.3

ASSEMBLY PROCESS FLOW

TAPE MOUNT WAFERS

↓

SAW

↓

GROSS INSPECTION

↓

PICK/PLACE/SORT

↓

EPOXY DIE ATTACH

↓

CURE

↓

WIRE BOND

↓

INSPECT/SORT

↓

EPOXY LID SEAL

↓

CURE

↓

BRAND

5.2.5.3 Packaging

A single standard die size (0.192" per side) has been chosen to permit standarization of package size and pin-out configuration. To accommodate custom and gate array designs and to utilize a cost effective packaging scheme, a 68 pin multilayer ceramic lead-less chip carrier with a 0.300" cavity will become the standard. Only the bond finger and external pad metalizations will be gold, with a substantial savings in package costs. As epoxy is being used for die attach and lid seal, no gold will be required in the die attach or seal ring areas. The standard pad ring configuration corresponding to the package described above will utilize the following layout rules:

Pad metal	100 microns X 100 microns
Passivation opening .	90 microns X 90 microns
Pad pitch	175 microns (Min)
Pad to adjacent metal	40 microns (Min)
Pad to active area. .	10 microns (Min)
Pad to scribe line. .	75 microns
Scribe line width . .	200 microns
Corner pads	none

These layout rules, depicted in Figure 5.2.4, were chosen to maximize operational efficiency in the assembly area, facilitating the automatic processing required for fast-turn fabrication.

FIGURE 5.2.4

LAYOUT RULES

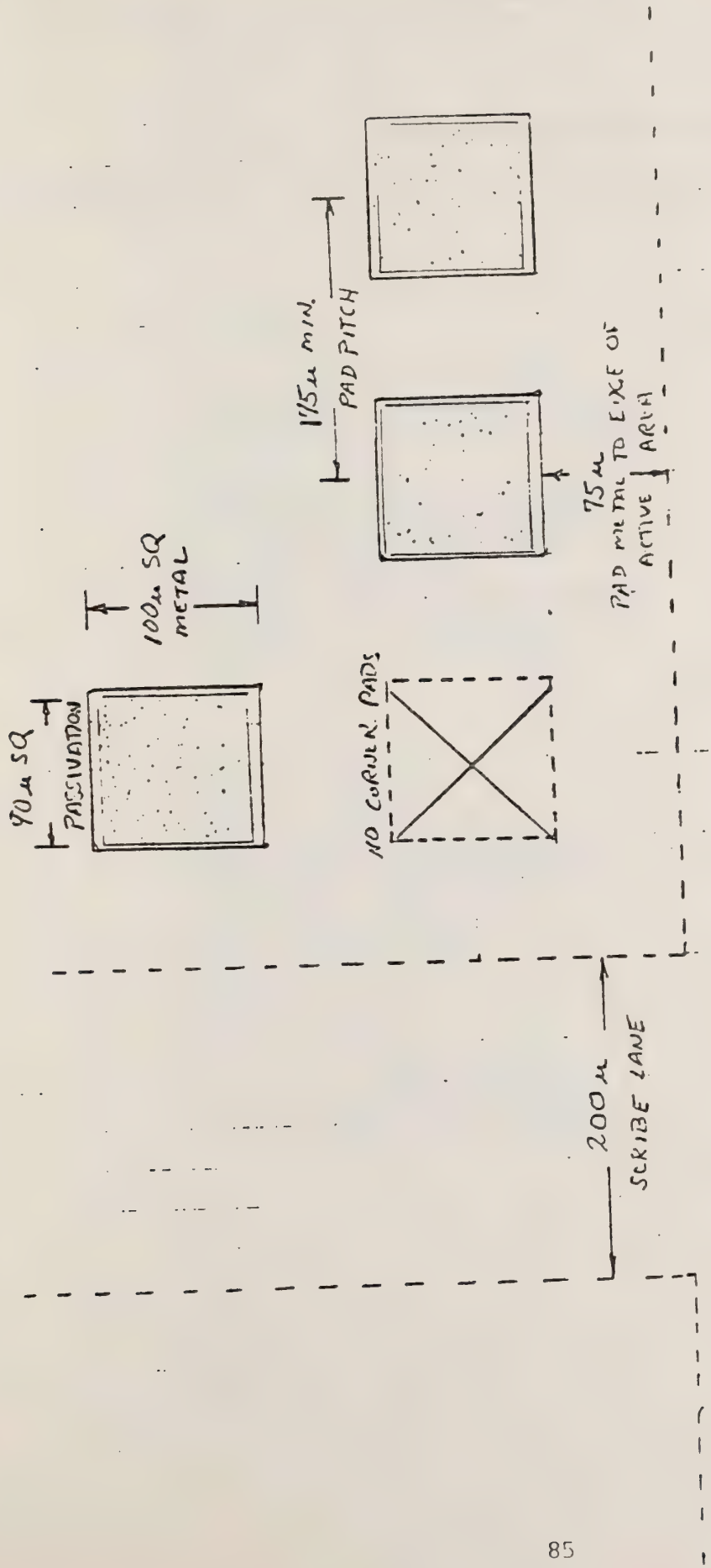


FIGURE 5
PAD RING LAYOUT

5.2.6 Equipment Requirements

The following key equipment requirements are critical to the establishment of a baseline fabrication facility.

Patterning	#	Fair Market Value	Total Value
Photoresist Coat Tracks	2	90,000	180,000
Projection Alignment Tools	2	700,000	1,400,000
Photoresist Dev./Bake Tracks	2	90,000	180,000
Dry Etch Tools	3	400,000	1,200,000
Plasma Photoresist Stripper	1	90,000	90,000
Acid Wafer Clean Station	1	100,000	100,000
Solvent Wafer Clean Station	1	80,000	80,000
Wet Etch Stations	2	90,000	180,000
Geometry Measurement System	1	60,000	60,000
Nanospec Film Thickness Meas.	1	60,000	60,000
Metallurgical Microscopes	4	15,000	60,000
TOTAL			3,590,000

Thermal Processing			
Furnace Tubes for High Temp. Operations and Reduced Pressure Depositions	16	89,375	1,430,000
Wafer Clean stations	1	200,000	200,000
Tube Cleaning Hood	1	50,000	50,000
Nanospec	1	60,000	60,000
Deglaze Station	1	60,000	60,000
Ellipsometer	1	24,000	24,000
Auxiliary Equipment for Measuring Film Thickness, Sheet Resistance, Junction Depths, & C-V Char.	1	200,000	200,000
TOTAL			2,024,000

Ion Implantation			
Med. Cur. Multi Source Impltr	1	730,000	730,000
RTA	1	115,000	115,000
Deglaze Station	1	60,000	60,000
TOTAL			905,000

Deposition	#	Fair Market Value	Total Value
AL-Si Sputtering System	1	250,000	250,000
Low Temperature CVD System for Final Glassivation	1	70,000	70,000
Leak Detector	1	12,000	12,000
Acid Wafer Clean Station	1	200,000	200,000
Solvent Wafer Clean Station	1	80,000	80,000
Deglaze Station	1	60,000	60,000
TOTAL			672,000
Test			
Wafer Probe System	1	100,000	100,000
Integrated WIP Tracking, Process Control, Comp. Sys.	1	500,000	500,000
TOTAL			600,000
Assembly			
Wafer Saw/Mount	1	100,000	100,000
Cleaning Station	1	10,000	10,000
Die Sort Station	1	35,000	35,000
Curing Ovens	2	5,000	10,000
Die Attach System	1	20,000	20,000
Auto Wire Bonders	1	95,000	95,000
Manual Wire Bonder	1	15,000	15,000
Microscopes	4	15,000	60,000
Dry Boxes, Laminar Flow Hoods	1	40,000	40,000
Branding System	1	1,000	1,000
TOTAL			386,000
Analytical Support			
Hoods	1	30,000	30,000
Scanning Electron Microscope	1	200,000	200,000
TOTAL			230,000
Equipment Maintenance			
Hoods	1	40,000	40,000
Diagnostic Tools	1	35,000	35,000
TOTAL			75,000

SUBTOTAL ICFF EQUIPMENT	8,482,000
INSTALLATION & FIT UP	1,200,000
	9,682,000
Fab Process Technology	2,100,000
Furniture & Accessories	175,000
GRAND TOTAL PERSONAL PROPERTY	11,957,000

5.2.7 Manpower Requirements

Conventional criteria relating to wafer fab productivity and efficiency do not apply in a fast turn low volume facility such as the Center Foundry. Staffing for the baseline Fabrication Facility must be predicated upon having sufficient manpower available to minimize wafer lot queuing. The following analysis is therefore based not on the most efficient use of manpower, but on the need to staff all areas to achieve short cycle time, for the wafer throughout requirements developed in this plan.

In the alignment area, one dedicated operator will be essential to maintain fast-turn throughput. Coating and developing can be handled by one operator. Two more operators would be required to inspect, etch, and strip this average daily wafer requirement, patterning silicon dioxide, polysilicon, silicon nitride, and aluminum - silicon. In addition to the

4 first shift operators, line support will be provided by 2 engineers, 2 process technicians and 2 equipment maintenance technicians. On second shift, one multiplexed operator performing a variety of tasks will be required.

Two operators will be needed to handle the number of individual furnace operations associated with the thermal processing/ion implantation area, including the associated wafer cleans and evaluations. A process technician will perform all ion implantations. Another process technician will support the high temperature processing area. Two equipment maintenance technicians will also be required. One engineer will support the entire area. On the second shift, one diffusion operator will be needed to maintain required lot throughput activities. In addition, a process technician will be available to operate the ion implanter and provide process engineering support throughout the wafer fab area. One equipment maintenance technician will be assigned to cover the entire wafer fab area on second shift.

One operator, one process technician, and one engineer will staff the thin film deposition area on first shift. In addition to the metalization and low temperature oxide processes of this area, the process engineer will also support the CVD operation in the thermal processing area. In the test/CAM area, one engineer and one computer technician will be responsible for DC parametric testing and defect density measurements as well as rudimentary screening of dice prior to assembly. In addition,

this group will maintain the central manufacturing computer network. This network will link all process areas directly to the central computer for wafer lot tracking and process control.

One equipment maintenance technician, one area supervisor, and three operators will be required to sustain assembly operations during peak loading periods. To maintain necessary throughput, a second shift will be necessary. It will be staffed by one equipment technician and one operator. To provide essential analytical support in SEM and both bulk and surface analysis, one engineer or one senior technician will be required. Chemical and gas handling, tube cleaning and repair, clean room garment control, and general supply functions will require one utility operator. Management will consist of the semiconductor operations manager and the following supervisory staff: one wafer fab process engineering manager, one equipment maintenance supervisor, one line supervisor, one second shift supervisor and a secretary.

Table 5.2.5 is a summary of the manpower detail described in this section along with an estimate, in Fiscal Year 1986 dollars, of position salaries. Table 5.2.5 includes an allocation of manpower by major functional area.

TABLE 5.2.5

Manpower Summary and Allocation[1]

	#	Annual Salary	Total Labor
Patterning			
Engineers	2	40,000	80,000
Process Technicians	2	25,000	50,000
Equipment Technicians	2	30,000	60,000
Operators	4	15,000	60,000
	10		250,000
Thermal Processing/Ion Implantation			
Engineer	1	40,000	40,000
Process Technician	2	25,000	50,000
Equipment Technicians	2	30,000	60,000
Operators	2	15,000	30,000
	7		180,000
Thin Film Deposition			
Engineer	1	40,000	40,000
Process Technician	1	25,000	25,000
Operator	1	15,000	15,000
	3		80,000
Test/CAM			
Engineer	1	40,000	40,000
Computer Technician	1	30,000	30,000
Operator	0	15,000	0
	2		70,000
Assembly			
Supervisor	1	30,000	30,000
Equipment Technician	1	30,000	30,000
Operator	3	15,000	45,000
	5		105,000
Analytical Support			
Engineer	1	40,000	40,000
	1		40,000

TABLE 5.2.5 (CONT'D)

Line Support	#	Annual Salary	Total Value
Technician	1	25,000	25,000
	1		25,000
Second Shift			
Shift Supervisor	1	33,000	33,000
Process Technicians	1	28,000	28,000
Equipment Technicians	2	33,000	66,000
Operators	3	17,000	51,000
	7		178,000
Management			
Process Engineering Manager	1	50,000	50,000
Line Supervisor	1	40,000	40,000
Equipment Maint. Supervisor	1	40,000	40,000
Secretary	1	20,000	20,000
	4		150,000
TOTAL	40		1,078,000

MANPOWER ALLOCATION

Wafer Fab:	24
Assembly:	5
MGM/SPV:	4
2nd Shift:	7
TOTAL	40

5.2.7.1 Fast Turn Operational Philosophy

As reviewed earlier, a fast-turn line should be staffed and equipped to minimize queuing. Due to budgetary constraints the equipment and manpower of the I.C. Foundry will be aggressively tasked to provide fast-turn cycle time. In providing minimum cycle times, the use of 24 hour operations is normally standard. In order to compensate for the lack of a full 3 shift operation, it is anticipated that the facility will apply some innovative variations in working hours in order to effect a smooth work flow, including skeleton crews assigned to back shift operations. In addition, periods of overtime work can be expected to compensate for unplanned down time or miscues.

Process control, essential to the success of any line will be even more important at MMC since functional testing will not be performed on-site. Only simple "go/no-go" testing will be performed on die. DC parametric testing of standard test patterns and testing of standard defect density patterns will be performed in conjunction with all VLSI design lots. Statistical process control principles will be applied to all unit processes throughout the line. Assurance of in-control operation will be attained by unit process control and DC testing of standard test groups present on all wafers processed in the line. In addition, even when no designs are being processed approximately

50 wafers (containing the necessary test patterns) will be started each week to insure a constant flow of silicon through the process.

It bears emphasis that for gate array designs, wafers will be stockpiled just prior to the personalization levels. From that point, wafers will be completed in about 1/3 of the time planned for full custom designs since eight (8) masking levels would have already been completed. The baseline Facility includes a favorable mix of custom and gate array designs to minimize the operating budget and the staffing levels of the Facility.

5.2.8 Operating Budget

The following budget (Table 5.2.6) is an estimate of the annual operating expenses, in Fiscal Year 1986 dollars, anticipated for the wafer throughput requirements developed in this plan. The budget detailed in Table 5.2.6 is predicated upon operating conditions required by the fabrication of the anticipated baseline number of designs per year. The start-up operational budget will be considerably less and will ramp-up only as the output capacity requirement increases.

TABLE 5.2.6

OPERATING BUDGET

Personnel	
Labor	1,078,000
Fringes	270,000
Peak Load overtime	86,000
	1,434,000
Materials	
E-Beam Masks	750,000
Silicon Substrates	55,000
Silicon Pilots	15,000
Packages	117,000
	937,000
Supplies	
Bulk Gases	108,000
Specialty Gases	160,000
Chemicals	120,000
Clean Rm. Supplies	20,000
Assembly Supplies	20,000
Spare Parts	300,000
Computer Supplies	12,000
Quartzware	24,000
Non-Capital Tools	10,000
Other Material	40,000
	814,000
Other	
Travel	25,000
Recruiting	25,000
Office Supplies	10,000
Miscellaneous	10,000
	70,000
Service Contracts	300,000
TOTAL	3,555,000

5.2.9 Expanded Operations

5.2.9.1 Introduction

The Fabrication Facility proposed in this Detailed Plan is a baseline Facility. Although the structure which will house the Fabrication Facility will be capable of supporting a substantial fabrication operation, the Facility itself is targeted at fabricating approximately 700 full custom designs and 1000 gate array designs annually. In adopting its baseline fabrication numbers, the Board considered that with an eighteen month construction schedule the Facility will not be capable of a fully operational baseline year until Fiscal Year 1989. It further considered that staffing the Facility, working with the technological process and equipment and integrating the facility's operation with the VLSI-CAD Network will involve a substantial degree of time and effort. Accordingly, the baseline target is deemed sufficient for the five year period (Fiscal Years 1987-1991) covered by the Plan.

The Board is committed to expanding the fabrication capacity of the Facility proposed in this Plan to the extent resources are made available for this purpose in subsequent years by industry and/or the State. It is the judgement of the Board that an expanded fabrication capacity will be warranted by an increase in university demands for fabrication services once the operation of the baseline Facility is fully integrated with

university instructional programs. The Board's plans include adding an internal photomask making component to the Facility. Under the baseline proposal, the Facility will employ a proprietary photomask foundry to manufacture the required masks. At the level of operation proposed for the baseline Facility, this is a cost-efficient means of securing masks. At any level of operation substantially in excess of the baseline, however, the expense of purchasing masks mitigates in favor of an internal mask making capacity. The requirements of a mask making component are reviewed below. Also included in the Board's plans are the addition of certain equipment items necessary to maintain the fast turn-around objective of the Fabrication Facility where the fabrication activity will be substantially increased. These equipment items and associated operational costs are reviewed separately below.

5.2.9.2 Mask Making

5.2.9.2.1 Justification

As the Fabrication Facility expands beyond its initial baseline operational level, the demand for increasing numbers of photomasks will grow significantly. The cost of purchasing photomasks from an external proprietary foundry will become prohibitively expensive. The operational costs associated with the expanded provision of fabrication services would be

substantially reduced through the addition of an internal mask making component to the Fabrication Facility.

5.2.9.2.2 Process Flow

The photomask blanks required for an internal mask making component will be obtained pre-coated with e-beam sensitive photoresist, alleviating the need for cleaning and coating mask blanks. Because numerous designs will be placed on the same mask, considerable time and manpower will be consumed in composing and formatting the data prior to e-Beam writing.

Standard critical dimension targets will be employed, independent of circuit designs to facilitate measurement of patterning accuracy. As with the baseline Facility, a standard die size will be employed. This will materially aid the cycle time goals by facilitating automatic inspection and registration checks. In addition to the standard die size, a standard bond pad layout will be employed. This will allow the same final passivation mask to be used on all mask sets. The net effect will be to reduce the total number of masks in a single level metal process from ten (10) to nine (9), and from twelve (12) to eleven (11) in a two metal level process.

Upon completion of e-beam writing, the photomask will then be processed through the development operation, followed by a plasma step to remove residual resist from patterned areas.

The next step is chromium etching to form the desired images on the photomask. Upon completion of this etch operation, the e-beam resist is stripped from the plate, and it is ready for cleaning and inspection. The inspection includes the automatic detection of defects, registration checking and the measurement of sample critical dimension patterns.

5.2.9.2.3 Budgetary Impact

The following equipment items are required for an internal mask making component to the Fabrication Facility:

Mask Making	#	Fair Market Value
E-Beam Mask Making System	1	2,541,000
Mask Developing Station	1	100,000
Mask Etching Station	1	20,000
Plasma Descum Etcher	1	30,000
Mask Inspection Station	1	820,000
Resist Strip Station	1	50,000
Mask Comparator	1	725,000
Oven	1	10,000
Mask Cleaning Station	1	50,000
	TOTAL	4,346,000

To staff the mask making component, the following additional personnel will be required:

E-Beam	#	Annual Salary	Total Labor
First Shift			
Engineers	2	40,000	80,000
Process Technicians	2	25,000	50,000
Operator	1	15,000	15,000
Second Shift			
Process Technicians	1	28,000	28,000
Operator	1	17,000	17,000
TOTAL	7		190,000

5.2.9.3 Additional Capacity

5.2.9.3.1 Increased Equipment Requirement

Increased operational levels will necessitate some expansion in the capital equipment base. The following is a list of the additional equipment needed for additional operations:

Patterning			
Dry Etch Tools	1	310,000	310,000
Wafer Inspection Systems	2	100,000	200,000
TOTAL			510,000
Thermal Processing			
Laser Marker	1	75,000	75,000
Chemical Delivery Systems	7	30,000	210,000
TOTAL			285,000
Deposition			
PE CVD System	1	300,000	300,000
TOTAL			300,000
Test			
Dice Screen Test System	1	500,000	500,000
TOTAL			500,000
Assembly			
Auto Wire Bonders	3	95,000	285,000
Branding System	1	30,000	30,000
TOTAL			315,000
Analytical Support			
X-Ray Flourescence Spectromet	1	100,000	100,000
Auger Electron Spectrometer	1	100,000	100,000
TOTAL			200,000
SUBTOTAL ICFF EQUIPMENT			2,110,000
INSTALLATION & FIT UP			300,000
GRAND TOTAL			2,410,000

5.2.9.3.2 Increased Staffing

Increased operational levels will necessitate the addition of the following personnel:

	#	Annual Salary	Total Labor
First Shift			
Operator	3	15,000	45,000
Second Shift			
Process Technicians	1	28,000	28,000
Operator	3	17,000	51,000
TOTAL	7		124,000

5.2.9.4 Expanded Operational Summary

Table 5.2.7 depicts the operating budget for the Integrated Circuit Fabrication Facility at the expanded operation level discussed above, including the addition of an internal mask making component. Table 5.2.7 also includes all Site Administration costs associated with an expanded operation level.

TABLE 5.2.7 Expanded Fabrication Facility Operating Budget

Personnel	
Labor	1,381,000
Fringes	359,000
Peak Load overtime	114,880
Consultants	0
	1,854,880
Materials	
E-Beam Mask Blanks	206,000
Silicon Substrates	82,500
Silicon Pilots	20,000
Packages	195,000
	503,500
Supplies	
Bulk Gases	120,000
Specialty Gases	180,000
Chemicals	140,000
Clean Rm. Supplies	26,000
E-Beam Processing	25,000
Assembly Supplies	25,000
Spare Parts	450,000
Computer Supplies	12,000
Quartzware	24,000
Non-Capital Tools	10,000
Other Material	40,000
	1,052,000
Other	
Travel	25,000
Recruiting	25,000
Office Supplies	10,000
Miscellaneous	10,000
	70,000
Service Contracts	485,000
Site Administration	
Labor	315,000
Fringes	78,750
Insurance	50,000
Utilities	950,000
Sup. & Cont. Serv.	120,000
Refuse	6,000
	1,519,750
TOTAL	5,485,130

EXHIBIT 5.2.1

DETAILED CMOS PROCESS FLOW

OPERATIONS	TIME (HRS.)	
	10 MASKS	12 MASKS
Lot Make-Up/ID	0.5	0.5
Wafer Clean	0.5	0.5
Well Masking Oxidation	2.5	2.5
N Well Patterning	3.5	3.5
Wafer Clean	0.5	0.5
N Well Implantation	0.2	0.2
Wafer Clean	0.5	0.5
N Well Diffusion	7.5	7.5
Initial Oxidation	2.5	2.5
Nitride Deposition	2.5	2.5
Nitride Patterning	3.5	3.5
Wafer Clean	0.5	0.5
N-Ch Field Implantation	0.2	0.2
P-Ch Field Patterning	3.5	3.5
P-Ch Field Implantation	0.2	0.2
Wafer Clean	0.5	0.5
Field Oxidation	6.0	6.0
1st Gate Oxidation	2.0	2.0
V_{TP} Implantation	0.2	0.2
V_{TN} Adj. Patterning	3.5	3.5
Wafer Clean	0.5	0.5

EXHIBIT 5.2.1 (CONT'D.)

DETAILED CMOS PROCESS FLOW (CONT;D.)

OPERATIONS	TIME (HRS.)	
	10 MASKS	12 MASKS
V_{TN} Adj. Ion Implantation	0.2	0.2
Wafer Clean	0.5	0.5
2nd Gate Oxidation	2.0	2.0
Polysilicon Deposition	3.0	3.0
Polysilicon Doping	1.0	1.0
Polysilicon Patterning	3.5	3.5
Wafer Clean	0.5	0.5
N^+ Source/Drain Patterning	3.5	3.5
N^+ Ion Implantation	0.4	0.4
Wafer Clean	0.5	0.5
S/D Reoxidation	2.0	2.0
P^+ Source/Drain Patterning	3.5	3.5
P^+ Ion Implantation	0.3	0.3
Wafer Clean	0.5	0.5
Field Oxide Deposition	1.5	1.5
Oxide Reflow	1.0	1.0
Wafer Clean	0.5	0.5
Contact Aperture Patterning	3.5	3.5
Wafer Clean	0.5	0.5
Metal 1 Deposition	2.0	2.0
Metal 1 Patterning	3.5	3.5
Wafer Clean	0.5	0.5

EXHIBIT 5.2.1 (CONT'D.)

DETAILED CMOS PROCESS FLOW CONT'D.)

OPERATIONS	TIME (HRS.)	
	10 MASKS	12 MASKS
*Dielectric Deposition	-	1.5
*Dielectric Patterning	-	3.5
*Wafer Clean	-	0.5
*Metal 2 Deposition	-	2.0
*Metal 2 Patterning	-	3.5
Sinter	1.5	1.5
Wafer Clean	0.5	0.5
Passivation Deposition	1.5	1.5
Passivation Patterning	3.5	3.5
Wafer Clean	0.5	0.5
Sub Total	83.2	94.2
Transfer Time	2.5	2.9
Measurements	1.1	1.2
GRAND TOTAL	86.8	98.3

*These processes, used in gate array fabrication, will not be utilized in full custom, fast-turn fabrication.

EXHIBIT 5.2.2

DESIGN/WAFER THROUGHPUT OPTIMIZATION

The following analysis[1] attacks the problem of optimizing the number of unique designs to be combined on a given mask set. It was performed for ten (10) wafer lots, with the goal of providing each designer with a minimum of five (5) potentially functional packaged units.

[1] Provided by D. Priore of Digital Equipment Corporation's Technology Group.

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 4 Maximum packaged die/design: 25

# Good Die	Probability	Cum Probability
0	0.520%	0.520%
1	2.362%	2.882%
2	5.871%	8.753%
3	10.317%	19.070%
4	14.194%	33.264%
5	16.112%	49.376%
6	15.558%	64.934%
7	13.011%	77.945%
8	9.522%	87.467%
9	6.129%	93.597%
10	3.476%	97.073%
11	1.736%	98.809%
12	0.762%	99.571%
13	0.293%	99.864%

Expectation: 5.67 Standard Deviation: 2.41

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 5 Maximum packaged die/design: 25

# Good Die	Probability	Cum Probability
0	0.211%	0.211%
1	1.037%	1.247%
2	2.936%	4.183%
3	6.058%	10.241%
4	9.958%	20.199%
5	13.585%	33.783%
6	15.694%	49.477%
7	15.513%	64.991%
8	13.194%	78.184%
9	9.686%	87.870%
10	6.150%	94.020%
11	3.380%	97.399%
12	1.608%	99.008%
13	0.662%	99.669%

Expectation: 6.60 Standard Deviation: 2.46

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 6 Maximum packaged die/design: 25

# Good Die	Probability	Cum Probability
0	0.103%	0.103%
1	0.539%	0.641%
2	1.726%	2.367%
3	4.100%	6.466%
4	7.736%	14.202%
5	11.934%	26.137%
6	15.291%	41.428%
7	16.445%	57.873%
8	14.965%	72.839%
9	11.596%	84.435%
10	7.687%	92.122%
11	4.374%	96.496%
12	2.141%	98.637%
13	0.902%	99.538%
14	0.326%	99.865%

Expectation: 7.07 Standard Deviation: 2.40

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 8 Maximum packaged die/design: 25

# Good Die	Probability	Cum Probability
0	0.041%	0.041%
1	0.249%	0.290%
2	0.995%	1.285%
3	2.859%	4.144%
4	6.245%	10.390%
5	10.731%	21.121%
6	14.875%	35.996%
7	16.952%	52.948%
8	16.109%	69.057%
9	12.900%	81.956%
10	8.773%	90.729%
11	5.094%	95.823%
12	2.534%	98.357%
13	1.081%	99.438%
14	0.396%	99.834%

Expectation: 7.39 Standard Deviation: 2.33

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 10 Maximum packaged die/design: 25

# Good die	Probability	Cum Probability
0	0.026%	0.026%
1	0.183%	0.209%
2	0.831%	1.041%
3	2.579%	3.619%
4	5.902%	9.521%
5	10.447%	19.969%
6	14.769%	34.738%
7	17.060%	51.798%
8	16.369%	68.167%
9	13.203%	81.370%
10	9.028%	90.398%
11	5.264%	95.662%
12	2.627%	98.290%
13	1.124%	99.414%
14	0.413%	99.826%

Expectation: 7.46 Standard Deviation: 2.31

EXHIBIT 5.2.2 (CONT'D)

Wafers/lot: 10 Die/design/wafer: 15 Maximum packaged die/design: 25

# Good die	Probability	Cum Probability
0	0.019%	0.019%
1	0.151%	0.170%
2	0.756%	0.926%
3	2.455%	3.381%
4	5.752%	9.133%
5	10.324%	19.457%
6	14.724%	34.181%
7	17.109%	51.290%
8	16.485%	67.774%
9	13.336%	81.111%
10	9.140%	90.251%
11	5.340%	95.591%
12	2.669%	98.260%
13	1.144%	99.403%
14	0.420%	99.823%

Expectation: 7.49 Standard Deviation: 2.29

5.3 Real Property

As of this date, the design effort on the facility intended to house the I.C. fabrication pieces of the M^2C, has been completed through the design phase. The following discussion (first presented in the MTPC detailed plan dated July 1, 1985) summarizes the product of those efforts. Relevant portions of the Design Development report are attached in Section 8.1.

The facility will be located in the open area at the top of the Lyman School grounds which is a 5 acre parcel between the Fish and Wildlife building and the present Cafeteria (future CAD) building. It will be a two story structure, with interstitial mechanical space, totaling approximately 70,900 square feet. The building "footprint" (square footage on grade) will be approximately 30,400 square feet. In addition to the building structure, there will be a small tankfarm in the rear for the house gas systems as well as storage bunkers for the various cylinder gases associated with the processes. A site map is attached as Exhibit 5.3.1

The first level of the new facility will consist of three primary sections: (1) entry level spaces and fabrication support; (2) process support, and; (3) mechanical support. The proposed entry level spaces and fabrication support areas include such areas as: a lobby, first aid and nurses' room, a janitor's room, fabrication facility staff offices, mechanical rooms for

non-process areas, a conference room, a computer room for production control, probe, assembly and test spaces, SEM/analytical room, security and reception, rest rooms, and other small associated areas.

The proposed process support space on the first level includes all below the fabrication support functions (including process equipment support) that require a hazardous occupancy rated area. This refers to gaseous and liquid chemical usages which are of a toxic, combustible or pyrophoric nature and which require transportation, storage and/or use in a protected fire-rated area. The following equipment and functions will be located in this section: all process equipment gas cabinets, process vacuum pumps, chemical storage (acids and solvents) and chemical mix, process equipment maintenance, and fume scrubbing systems.

The rear third of the proposed facility will house the mechanical support spaces required. This section of the building will be constructed on an independent foundation system and will be tied to the front two thirds of the structure with flexible expansion joints. The reason for this treatment is to avoid transmission of harmful vibration from the mechanical equipment to the sensitive process equipment that will be in use. The mechanical equipment mentioned includes: boilers, chillers, high and low vacuum systems, house vacuum system, compressed air systems, de-ionized water systems, waste water pre-treatment

systems and cooling tower pumps, as well as a separate electrical room for the control and distribution of power to the facility.

The second level of the proposed new facility (30,200 sq. ft. total) consists of two primary space clean rooms for I.C. fabrication with associated cleanroom support spaces, and two HVAC/mechanical space. The proposed clean room fabrication areas consist of eight clean fabrication "bays", each capable of achieving class 100 cleanliness levels or better. Six bays are dedicated for the Integrated Circuit Foundry and two for mask making and processing.

As the structure is intended initially to support a baseline Fabrication Facility, the two bays identified for mask making will be left unfinished. Items related to those two bays will be deferred until the determination is made to include an internal mask making component to the Fabrication Facility. Those items include: transfer fans and all related HVAC and duct equipment, demountable wall systems, filtered ceiling systems, consductive floorings, electrical support wiring and all process liquid and gas piping. The total clean room area under High Efficiency Particulate Air (HEPA) filtration is approximately 6,800 square feet. Intermingled with the clean spaces are the associated service chases, service aisles, corridors, and process support spaces. The entire process floor referenced will be structurally isolated from the remainder of the facility to insure a vibration free environment for the sensitive processes.

The sizing for the clean spaces was derived from an equipment list designed to support the required production levels as described in Section 5.2. A lounge, gowning area, rest rooms, non-clean room mechanical space, and circulation corridors are on this level as support spaces for the process areas.

In the rear of the second level will be the HVAC/mechanical space. This area will consist mainly of make-up air handling units and the main mechanical control panels for the building operations. Super-imposed directly above this space will be an interstitial area (10,300 square feet) which will house 16 vane axial fan units capable of up to 50,000 CFM each. These will comprise the main air circulation system for the fabrication areas. It will be necessary to change the entire volume of air in the cleanrooms every 6 seconds and maintain temperatures within 1/2°F and humidity levels to a 2-1/2% R.H. range.

The facility will be protected by state-of-the-art fire and smoke detections systems along with automatic sensing for gas and liquid leaks. Also, the building environment, which is to be held to a very tight climatalogical tolerances, will be monitored by computer and capable of real-time self-diagnostics to avoid costly shutdowns due to an "out-of spec" condition. All critical systems (re: fire, smoke, toxic leaks, security) will be monitored around the clock at a centralized enunciator panel. Fire and toxic leak alarms will also go directly to the

Westborough Fire Department (WFD). A comprehensive training and information exchange program will be developed with the WFD and local medical services to insure their ability to deal with any emergency that could arise at the Center.

Space allocation breakdowns are attached as Exhibit 5.3.2. A construction cost estimate in provided in Exhibit 5.3.3. A review of increases in Site Administration staff and operating expenses are included as Exhibits 5.3.4 and 5.3.5. Finally, a Capital Facilities Budget is attached as Exhibit 5.3.6

EXHIBIT 5.3.1

SITE MAP

[TO BE INSERTED]

SECOND DETAILED PLAN EXHIBIT 5.3.1 6/18/80

Descriptive Materials Subsection
Real Property Division

EXHIBIT 5.3.2

Semiconductor Building

SPACE BREAKDOWN

First Floor Areas	Sq. Ft.
Offices	-
Mechanical	6,840
P. E. Maintenance	-
Lobby	567
Vestibule	96
Coats	96
Lockers	96
Stairs	128
Fab Support	5,690
HPM Storage	1,269
P. E. Support	10,414
Receiving	624
Scrubber	820
Mechanical	-
Electrical	-
Process Support	-
Service Elevator	150
Elevator	48
Service Yard	-
Bulk Gas Storage	-
Pryo Storage	-
Conference	-
Nursing Office	378
Health Room	-
Reception/Security	357
Waiting	-
Men	194
Women	194
Stair (N&S, 1&2)	972
	28,933
Misc., Circulation and Wall Thickness	1,480
Footprint of 1st Floor*	30,413

Second Floor Area

Gown	537
First Dressing	213
Mechanical	337
Secretary	112
Office	130
Lounge	732
Men	151

Exhibit 5.3.2 (continued)

Second Floor Areas		Sq. Ft.
Women		162
Elevator		55
Clean Corridor	1,004	
Clean Bay	5,824	
Service Area	2,196	
Chase	4,513	14,070
Egress Corridor]		
MU-Air Storate]		
Service Elevator }		8,346
Elevator Equipment]		
Stair]		
Meeting		0
Interview		0
Conference #1		275
Conference #2		275
Office		118
Office		118
Office		136
Office		64
Office		64
Office		64
Office		64
Open Office		1,227
Stair (N&S, 1&2		972
		28,222
Circulation and Wall Thickness		1,978
Footprint of Second Floor		30,200

Third Floor Plan	
Mechanical	9,654
Service Elevator	160
Stair (N&S)	486
Footprint of Third Floor*	10,300

Summary	
First Level	30,413
Second Level	30,200
Third Level	10,300
Total	70,913

* Footprint of floor is gross area.

Exhibit 5.3.3

Semiconductor Building

CONSTRUCTION COST ESTIMATE

Category			Filed Subbid
Masonry			479,300
Miscellaneous Steel & Metal			168,900
Single Ply Roofing			78,900
Sealants			10,300
Metal Windows			62,600
Glass & Glazing			17,000
Ceramic Tile			10,000
Acoustical Ceiling			34,500
Resilient Flooring			93,300
Painting			82,400
Plumbing			1,133,000
HVAC			3,381,600
Sprinklers			131,400
Electrical			1,178,800
Elevators			124,400
		Total	6,986,400
	LESS:	Mask Making & Desireables	596,000
		Total Filed Subbid	6,390,400
	ADD:	G.C. Contract Sell	2,445,795
		Total Construction Cost	8,836,195
	ADD:	G.C. Markup @ 7%	618,534
		Total Construction & G.C. Fees	9,454,729
	ADD:	Engineering/Architectural Fees	730,000
	ADD:	Engineering/Architectural Reimbursable Expenses	25,000
		GRAND TOTAL	10,209,729

EXHIBIT 5.3.4

Semiconductor Building

SITE ADMINISTRATION STAFFING PLAN

-	Environmental Health Safety Engineer/Industrial Hygienist	1
-	Mechanics (Facilities)	2
-	Mechanic (Process)	1
-	Custodian	1
-	Chemical Handler	1
-	Nurse	1
-	Electrician	1
-	Security	3
		11

EXHIBIT 5.3.5

Semiconductor Building

Site Administration Costs

(000's)

Summary

Staff		
Salary		315.00
Fringe Benefits		78.75
	Total	393.75
Operating Expenses		
Waste Removal		6.00
Supplies/Maintenance/Management		120.00
Insurance		50.00
Utilities		870.00
	Total	1,046.00
	Grand Total	1,439.75

EXHIBIT 5.3.6

Semiconductor Building

CAPITAL FACILITIES BUDGET

(000's)

1)	Construction Costs		
	- New Facility	$8,836.2	
	- TOTAL Costs		$ 8,836.2
2)	Design and Construction Fees		
	- Engineering/Architectural Fees	730.0	
	- Engineering/Architectural Reimbursable Expenses	25.0	
	- General Contractor Fees @ 7%	618.5	
	TOTAL Design and Construction Fees		1,373.5
	GRAND TOTAL Capital Facilities Budget		$10,209.7

5.4 Budgetary Materials

5.4.1 Introduction

The Budgetary Materials subsection of the Second Detailed Plan has three divisions: a Project Cost (capital cost) division (Section 5.4.2); an Operating Cost division (Section 5.4.3); and a division which specifically requests State capital and operating funds from the State in support of the Second Phase of the center project (Section 5.4.4). This subsection follows from the educational and facilities programs contained in Sections 5.2 and 5.3 of this document.

As this document is a planning document, the capital and operating budgets contained herein were developed and are expressed subject to a number of guidelines. Guidelines specific to a particular division are discussed in detail in that division. There are, however, a number of general guidelines which serve to establish a frame of reference for the entire Budgetary Materials subsection and are deserving of an initial review.

The first general guideline reflects the approach adopted by the Board of Directors in preparing the educational, facilities and operational plans for the Second Phase of the Center. The Board has carefully defined the foregoing in terms of minimum objectives and threshold activities. Accordingly, the

capital and operating budgets contained in this subsection are specifically represented as the minimum necessary to support the Integrated Circuit Fabrication Facility element of the Center. Additional objectives, facilities and activities are not precluded by this Detailed Plan. Requests in subsequent years for additional State funds in support of the Fabrication Facility, if any, are to be presented as optional, divisible items for review and consideration as a part of the normal budgetary process.

The second general guideline concerns the nature of a detailed plan for a center under the Corporation's enabling act. Section 6(b) of Chapter 40J requires the Corporation to develop what is essentially a five year business plan for a center. As with any business plan, it is both measured and limited by the extent to which it is predicated upon a thorough analysis of available information and reasonably forseeable changes in circumstances. The more thorough the analysis, the more accurate the business plan is as a guide to actual operations and the less of a risk is imposed upon the parties to the center partnership. It is proposed that this Second Detailed Plan for the Massachusetts Microelectronics Center is based on the desired degree of analysis and forethought. Yet this Plan and its Budgetary Materials are nonetheless only presented as a guide to the Center's proposed operations. The actual operation of the Center, and with it the level of necessary public funding, could deviate to a certain degree from that proposed in the Plan.

Further, unanticipated and unforseeable changes in circumstances can and do occur, with concomitant implications for operational ad budgetary plans. In general, a business plan is intended to minimize the risks of an enterprise, it should not be viewed as eliminating that risk.

The final general guideline influencing the Center's Budgetary Materials subsection is that all cost and appropriation figures are expressed in terms of 1986 dollars. Adjustments for inflation will be made by the Board of Directors through annual maintenance funding requests. It is proposed that, so qualified, the Center's budget figures provide that State with a reasonable projection of anticipated costs.

5.4.2 Project Cost Budgets

Section 6(a)(1) of Chapter 40J requires that a detailed plan for a Center include "a statement of the project costs associated with establishing such a center, with a detailed breakdown of such project costs..." "Project Costs" are defined by Section 2 of Chapter 40J as the capital expenses of a center. Section 2 establishes seven categories of Project Costs: (1) construction costs; (2) land acquisition costs; (3) personal property acquisition costs; (4) site work costs; (5) finance charges; (6) design and construction fees and (7) other expenses.

Section 6(a)(2) prescribes that a detailed plan specify a center's Project Costs "for the first five years of its existence." The phrase "for the first five years of its existence" is defined for the purposes of this Detailed Plan as the period from Fiscal Year 1987 up to and including Fiscal Year 1991. The Corporation's Fiscal Year is identical to that of the State: July to June. Section 6(a)(2) provides further that a detailed plan for a center must include "a reasonable projection of that portion of [the Project Costs of a center] which the [C]orporation expects to meet through assistance provided by participating businesses, rates, rents, fees and charges imposed upon users and support from any other source." Similarly, Section 6(a)(3) of Chapter 40J requires that a detailed plan include "a description of the assistance to be provided to the

[C]orporation in support of the center by participating businesses and participating institutions."

Table 5.4.2.1 provides a complete statement of the Project Costs associated with the Second Phase of the Center, divided by appropriate category, and allocated by Fiscal Year and between the State and industry participants in the Center partnership. Participating universities are providing no capital assistance to the Second Phase of the Center. Tables 5.4.2.1.1 and 5.4.2.1.2 provide materials supplementary to the Project Cost Budget contained in Table 5.4.2.1. Table 5.4.2.1.1 details the anticipated construction costs associated with the Semiconductor Building and includes a statement of the design and construction fees associated with the building. The table was taken from Section 5.3 of this Plan. Table 5.4.2.1.2 contains the anticpated cost of the equipment and machinery required for the Fabrication Facility. The cost of the scientific equipment and machinery is stated in terms of its fair market value. This table was taken from Section 5.2 of this Plan.

The industry contribution figures contained in Table 5.4.2.1 include contributions which the Corporation expects to receive from industry before the Fabrication Facility is operational. Because the industry contribution figures include expectations, it is necessary: (1) to demonstrate that the capital funds which the Corporation is requesting from the State to construct the Fabrication Facility pursuant to this Plan are

currently matched by industry contributions for the total Center project; and (2) to clearly disclose the amount of additional donations which the Corporation must secure to make the Fabrication Facility operational. Table 5.4.2.2 compares the total of industry contribution commitments secured to date for the Center project with the aggregate of State capital funds requested for the Center in the First and Second Detailed Plans. Table 5.4.2.3 reviews the additional industry contributions which the Corporation expects to secure, and must secure, if it is to make the Fabrication Facility operational.

TABLE 5.4.2.1
Project Cost Budget

	1986-87 Budget	1987-88 Budget	1988-89 Budget	1989-90 Budget	1990-91 Budget	Total Budget
Construction						
STATE	3,534,478	5,301,717	0	0	0	8,836,195
INDUSTRY	0	0	0	0	0	0
	3,534,478	5,301,717	0	0	0	8,836,195
Land Acquisition						
STATE	0	0	0	0	0	0
INDUSTRY	0	0	0	0	0	0
	0	0	0	0	0	0
Personal Prop. Acq.						
STATE	650,523	2,602,092	0	0	0	3,252,615
INDUSTRY	1,740,877	6,963,508	0	0	0	8,704,385
	2,391,400	9,565,600	0	0	0	11,957,000
Site Work						
STATE	0	0	0	0	0	0
INDUSTRY	0	0	0	0	0	0
	0	0	0	0	0	0
Finance Costs						
STATE	0	0	0	0	0	0
INDUSTRY	0	0	0	0	0	0
	0	0	0	0	0	0
Design & Const. Fees						
STATE	650,000	289,414	434,120	0	0	1,373,534
INDUSTRY	0	0	0	0	0	0
	650,000	289,414	434,120	0	0	1,373,534
Summary						
STATE	4,835,001	8,193,223	434,120	0	0	13,462,344
INDUSTRY	1,740,877	6,963,508	0	0	0	8,704,385
TOTAL	6,575,878	15,156,731	434,120	0	0	22,166,729

TABLE 5.4.2.1.1

Project Cost Budget: Supporting Materials

Construction Cost Estimate

Category		Filed Subbid
Masonry		479,300
Miscellaneous Steel & Metal		168,900
Single Ply Roofing		78,900
Sealants		10,300
Metal Windows		62,600
Glass & Glazing		17,000
Ceramic Tile		10,000
Acoustical Ceiling		34,500
Resilient Flooring		93,300
Painting		82,400
Plumbing		1,133,000
HVAC		3,381,600
Sprinklers		131,400
Electrical		1,178,800
Elevators		124,400
	Total	6,986,400
LESS:	Mask Making & Desireables	596,000
	Total Filed Subbid	6,390,400
ADD:	G.C. Contract Sell	2,445,795
	Total Construction Cost	8,836,195
ADD:	G.C. Markup @ 7%	618,534
	Total Construction & G.C. Fees	9,454,729
ADD:	Engineering/Architectural Fees	730,000
ADD:	Engineering/Architectural Reimbursable Expenses	25,000
	GRAND TOTAL	10,209,729

TABLE 5.4.2.1.2
Project Cost Budget: Supplementary Materials (cont.)
Fabrication Facility Equipment Costs

	#	Fair Market Value	Total Value
Patterning			
Photoresist Coat Tracks	2	90,000	180,000
Projection Alignment Tools	2	700,000	1,400,000
Photoresist Dev./Bake Tracks	2	90,000	180,000
Dry Etch Tools	3	400,000	1,200,000
Plasma Photoresist Stripper	1	90,000	90,000
Acid Wafer Clean Station	1	100,000	100,000
Solvent Wafer Clean Station	1	80,000	80,000
Wet Etch Stations	2	90,000	180,000
Geometry Measurement System	1	60,000	60,000
Nanospec Film Thickness Meas.	1	60,000	60,000
Metallurgical Microscopes	4	15,000	60,000
TOTAL			3,590,000
Thermal Processing			
Furnace Tubes for High Temp. Operations and Reduced Pressure Depositions	16	89,375	1,430,000
Wafer Clean stations	1	200,000	200,000
Tube Cleaning Hood	1	50,000	50,000
Nanospec	1	60,000	60,000
Deglaze Station	1	60,000	60,000
Ellipsometer	1	24,000	24,000
Auxiliary Equipment for Measuring Film Thickness, Sheet Resistance, Junction Depths, & C-V Char.	1	200,000	200,000
TOTAL			2,024,000
Ion Implantation			
Med. Cur. Multi Source Impltr	1	730,000	730,000
RTA	1	115,000	115,000
Deglaze Station	1	60,000	60,000
TOTAL			905,000
Deposition			
AL-Si Sputtering System	1	250,000	250,000
Low Temperature CVD System for Final Glassivation	1	70,000	70,000
Leak Detector	1	12,000	12,000
Acid Wafer Clean Station	1	200,000	200,000
Solvent Wafer Clean Station	1	80,000	80,000
Deglaze Station	1	60,000	60,000
TOTAL			672,000

TABLE 5.4.2.1.2 (cont'd)
Project Cost Budget: Supplementary Materials (cont.)
Fabrication Facility Equipment Costs

Test	#	Fair Market Value	Total Value
Wafer Probe System	1	100,000	100,000
Integrated WIP Tracking, Process Control, Comp. Sys.	1	500,000	500,000
TOTAL			600,000
Assembly			
Wafer Saw/Mount	1	100,000	100,000
Cleaning Station	1	10,000	10,000
Die Sort Station	1	35,000	35,000
Curing Ovens	2	5,000	10,000
Die Attach System	1	20,000	20,000
Auto Wire Bonders	1	95,000	95,000
Manual Wire Bonder	1	15,000	15,000
Microscopes	4	15,000	60,000
Dry Boxes, Laminar Flow Hoods	1	40,000	40,000
Branding System	1	1,000	1,000
TOTAL			386,000
Analytical Support			
Hoods	1	30,000	30,000
Scanning Electron Microscope	1	200,000	200,000
TOTAL			230,000
Equipment Maintenance			
Hoods	1	40,000	40,000
Diagnostic Tools	1	35,000	35,000
TOTAL			75,000
SUBTOTAL ICFF EQUIPMENT			8,482,000
INSTALLATION & FIT UP			1,200,000
			9,682,000
Fab Process Technology			2,100,000
Furniture & Accessories			175,000
GRAND TOTAL PERSONAL PROPERTY			11,957,000

TABLE 5.4.2.2

Contributions Received: Toward Match and Project Costs

CORPORATE DONATIONS	TOWARD MATCH	TOWARD PROJECT COSTS
Analog Devices *	225,000	225,000
Cameo Systems	385,000	385,000
Canon	700,000	700,000
Data General	1,275,000	1,275,000
Digital Equipment Corporation	5,141,000	4,941,000
Drytek	650,000	650,000
E G & G	50,000	50,000
FSI Corporation	411,050	411,050
Hewlett Packard	113,434	0
Inficon	12,900	12,900
Ionic	400,000	150,000
KTI Chemicals Incorporated	14,000	14,000
LAM Research	300,000	300,000
Materials Research Corporation	250,000	250,000
MTI	360,000	360,000
Northern Telecom	75,000	0
Plasma Therm	90,000	90,000
Polaroid **	300,000	300,000
Prime	3,609,000	3,609,000
PWS	35,000	35,000
Raytheon	300,000	300,000
Varian	2,712,000	845,000
VLSI Technology Inc.	3,935,000	3,935,000
	21,343,384	18,837,950

AMOUNT IN EXCESS OF INDUSTRY MATCH REQUIREMENT $1,343,384

* represents verbal commitment
** represents anticipated commitment

TABLE 5.4.2.3
Total Project Costs Budget Shortfall

PHASE I PROJECT COSTS		
Construction, Renovations & Site Work	4,144,800	
Personal Property Acquisition	15,776,300	
Design & Construction Fees	935,500	
TOTAL PHASE I	20,856,600	
PHASE II PROJECT COSTS		
Construction, FAB Facility	8,836,195	
Personal Property Acquisition	11,957,900	
Design & Construction Fees	1,373,534	
TOTAL PHASE II	22,167,629	
A. TOTAL PHASE I & II PROJECT COSTS		43,024,229
STATE FUNDING TOWARD PROJECT COSTS		
PHASE I	6,537,656	
PHASE II (Requested, less State funds to be used for equipment purchases)	10,209,729	
	16,747,385	
DONATIONS TOWARD PROJECT COSTS		
PHASE I & PHASE II	18,837,950	
B. TOTAL FUNDING & DONATIONS TOWARD PROJECT COSTS		35,585,335
SUBTOTAL FUNDING SHORTAGE (A - B)		7,438,894
LESS:		
DEC or VTI Commitment for Technology Transfer	2,100,000	
		5,338,894
LESS:		
Fixed Installation & Fitup Costs	2,500,000	
		2,838,894
LESS:		
Value of Industry Discounts	709,724	
		2,129,171
ADD:		
Fixed Installation & Fitup Costs	2,500,000	
		4,629,171
LESS:		
State Funds Available for Equipment/Project Costs	3,252,615	
TOTAL PROJECT COSTS BUDGET SHORTFALL		1,376,556

5.4.3 Operating Budgets

Section 6(a)(1) of Chapter 40J requires that a detailed plan for a Center include "a statement of the proposed annual start-up expenses...and current expenses of the center for the first five years of its existence, including a detailed breakdown of such ...expenses..." The terms "start-up expenses" and "current expenses" are defined pursuant to Section 2 of Chapter 40J to be the annual operational expenses of a center for the period before and after it becomes operational, respectively. As with the Project Cost Budget, the phrase "for the first five years of its existence" is defined as the period from Fiscal Year 1987 up to and including Fiscal Year 1991. The Corporation's Fiscal Year is identical to that of the State: July to June.

Section 6(a)(2) provides further that a detailed plan for a center must include "a reasonable projection of that portion of [the Project Costs of a center] which the [C]orporation expects to meet through assistance provided by participating businesses, rates, rents, fees and charges imposed upon users and support from any other source." Similarly, Section 6(a)(3) of Chapter 40J requires that a detailed plan include "a description of the assistance to be provided to the [C]orporation in support of the center by participating businesses and participating institutions."

Table 5.4.3.1 provides a statement of the projected annual operating expenses of the Second Phase of the Center, allocated among the parties to the Center partnership and by Fiscal Year. The State participation refers to the annual appropriation required to support the Second Phase of the Center for the specified Fiscal Year. University contributions are to be in the form of charges paid per student-designed circuit which is manufactured by the Fabrication Facility. Industry contributions are in the form of discounted supplies and materials. Table 5.4.3.1.1 explains the additional manpowers expenses associated with Phase II of the Center, while Table 5.4.3.1.2 provides a more detailed review of the total operating expenses of the Center's Second Phase by Fiscal Year. Tables 5.4.3.1.1 and 5.4.3.1.2 were derived from Sections 5.2 and 5.3 of this Detailed Plan. The two basic categories of operating expenses are the Integrated Circuit Fabrication Facility and Site Administration.

It bears mentioning that the Board of Directors was extremely reluctant to include significant revenue projections or donations of operational support from industry in its Operating Budget. With regard to revenue which the Fabrication Facility may be expected to generate, the Board is committed both to vigorously pursuing such revenue and to using any revenue generated by the Fabrication Facility to defray the need for an annual appropriation from the State. However, it was considered speculative at best to include projections of revenue as an

essential element of the Operating Budget at this time. Possible revenue generating activities of the Fabrication Facility involve serving as a beta testing site for industry, serving as the host facility for innovative industry-university research projects, and fabricating circuits for the students and faculty of universities from outside the Commonwealth. So too with donations of annual operating support from industry. The Center will be actively soliciting contributions of supplies, technical assistance and direct financial support from industry and expects that its requests will be favorably received. Yet commitments to provide operational support over a significant time period are more susceptible than one time capital equipment contributions to changes in circumstances. Accordingly, the Board has not included a major reliance upon industry operating donations, particularly donations of money, in its Operating Budget for the Second Phase of the Center.

TABLE 5.4.3.1

Five Year Operating Budget

	1986-87 Budget	1987-88 Budget	1988-89 Budget	1989-90 Budget	1990-91 Budget
ICFF					
STATE	206,250	2,101,000	2,895,000	2,895,000	2,895,000
UNIVERSITY	0	90,000	340,000	340,000	340,000
INDUSTRY	0	160,000	320,000	320,000	320,000
	206,250	2,351,000	3,555,000	3,555,000	3,555,000
Site Administration					
STATE	0	652,275	1,439,750	1,439,750	1,439,750
UNIVERSITY	0	0	0	0	0
INDUSTRY	0	0	0	0	0
	0	652,275	1,439,750	1,439,750	1,439,750
Summary					
STATE	206,250	2,753,275	4,334,750	4,334,750	4,334,750
UNIVERSITY	0	90,000	340,000	340,000	340,000
INDUSTRY	0	160,000	320,000	320,000	320,000
TOTAL	206,250	3,003,275	4,994,750	4,994,750	4,994,750

ICFF

Includes total labor and non-labor costs for the ICFF with partial operational year in Fiscal Years 1988 and operating at baseline capacity thereafter. This operational level will support up to 700 full custom and 1000 gate array designs per year. State costs are to be in support of the ICFF, including both labor and non-labor costs. University costs arise from the $200/Design fee. Operational costs to the ICFF element of the center allocated to industry represent estimated discounts.

Site Administration

Includes both labor and non-labor costs for site administration. First full operational year is targeted for Fiscal Year 1988, with Fiscal Years 1990-91 remaining at a steady state. All costs of administering the facility are allocated to the State.

TABLE 5.4.3.1.1
Operating Budget: Supplementary Materials (cont.)

Manpower Summary

Fabrication Facility

Patterning	#	Annual Salary	Total Labor
Engineers	2	40,000	80,000
Process Technicians	2	25,000	50,000
Equipment Technicians	2	30,000	60,000
Operators	4	15,000	60,000
	10		250,000
Thermal Processing/Ion Implantation			
Engineer	1	40,000	40,000
Process Technician	2	25,000	50,000
Equipment Technicians	2	30,000	60,000
Operators	2	15,000	30,000
	7		180,000
Thin Film Deposition			
Engineer	1	40,000	40,000
Process Technician	1	25,000	25,000
Operator	1	15,000	15,000
	3		80,000
Test/CAM			
Engineer	1	40,000	40,000
Computer Technician	1	30,000	30,000
Operator	0	15,000	0
	2		70,000
Assembly			
Supervisor	1	30,000	30,000
Equipment Technician	1	30,000	30,000
Operator	3	15,000	45,000
	5		105,000
Analytical Support			
Engineer	1	40,000	40,000
			40,000
Line Support			
Technician	1	25,000	25,000
	1		25,000

Second Shift	#	Annual Salary	Total Labor
Shift Supervisor	1	33,000	33,000
Process Technicians	1	28,000	28,000
Equipment Technicians	2	33,000	66,000
Operators	3	17,000	51,000
	7		178,000
Management			
Process Engineering Manager	1	50,000	50,000
Line Supervisor	1	40,000	40,000
Equipment Maint. Supervisor	1	40,000	40,000
Secretary	1	20,000	20,000
	4		150,000
TOTAL	40		1,078,000

Site Administration

	#	Annual Salary	Total Labor
Env. Health Safety Eng.	1	45,000	45,000
Nurse	1	22,000	22,000
Facility Mechanic	2	30,000	60,000
Process Mechanic	1	35,000	35,000
Custodian	1	18,000	18,000
Chemical Handler	1	25,000	25,000
Security Guard	3	25,000	75,000
Electrician	1	35,000	35,000
TOTAL	11		315,000

TABLE 5.4.3.1.2
Operating Budget: Supplementary Materials (cont.)
Operating Budget Summary

Integrated Circuit Fabrication Facility

Personnel	1986-87 Budget	1987-88 Budget	1988-89 Budget	1989-90 Budget	1990-91 Budget
Labor	45,000	820,000	1,078,000	1,078,000	1,078,000
Fringes	11,250	205,000	270,000	270,000	270,000
Peak Load overtime	0	0	86,000	86,000	86,000
Consult./Start Up	60,000	300,000	0	0	0
	116,250	1,325,000	1,434,000	1,434,000	1,434,000
Materials					
E-Beam Masks	0	225,000	750,000	750,000	750,000
Silicon Substrates	0	25,000	55,000	55,000	55,000
Silicon Pilots	0	5,000	15,000	15,000	15,000
Packages	0	45,000	117,000	117,000	117,000
	0	300,000	937,000	937,000	937,000
Supplies					
Bulk Gases	0	40,000	108,000	108,000	108,000
Specialty Gases	0	60,000	160,000	160,000	160,000
Chemicals	0	45,000	120,000	120,000	120,000
Clean Rm. Supplies	0	8,000	20,000	20,000	20,000
E-Beam Processing	0	0	0	0	0
Assembly Supplies	0	10,000	20,000	20,000	20,000
Spare Parts	0	120,000	300,000	300,000	300,000
Computer Supplies	0	4,000	12,000	12,000	12,000
Quartzware	0	9,000	24,000	24,000	24,000
Non-Capital Tools	0	4,000	10,000	10,000	10,000
Other Material	0	16,000	40,000	40,000	40,000
	0	316,000	814,000	814,000	814,000
Other					
Travel	0	0	25,000	25,000	25,000
Recruiting	90,000	210,000	25,000	25,000	25,000
Office Supplies	0	0	10,000	10,000	10,000
Miscellaneous	0	0	10,000	10,000	10,000
	90,000	210,000	70,000	70,000	70,000
Service Contracts	0	200,000	300,000	300,000	300,000
Site Administration					
Labor	0	157,500	315,000	315,000	315,000
Fringes	0	39,375	78,750	78,750	78,750
Insurance	0	25,000	50,000	50,000	50,000
Utilities	0	380,000	870,000	870,000	870,000
Sup. & Cont. Serv.	0	48,000	120,000	120,000	120,000
Refuse	0	2,400	6,000	6,000	6,000
	0	652,275	1,439,750	1,439,750	1,439,750
TOTAL	206,250	3,003,275	4,994,750	4,994,750	4,994,750

5.4.4 State Action Requested

Section 6(a)(6) of Chapter 40J provides that a detailed plan for a center must include: "a proposal for a capital outlay appropriation from the [C]ommonwealth in support of the establishment of the center and such annual maintenance appropriations as may reasonably be required for the successful operation of the center..." This Budgetary Materials division contains a proposal for a capital outlay appropriation in subdivision 5.4.4.1 and proposals for annual maintenance appropriations in subdivision 5.4.4.2. These proposals are expressly made subject to the general guidelines contained in this Budgetary Materials subsection.

5.4.4.1 Capital Outlay Appropriation

The Corporation requests no additional capital outlay appropriation from the Commonwealth in support of the Center. The Corporation does request that the sum of $13,462,344 be allocated to the Corporation from the monies previously appropriated pursuant to Chapter 327 of the Acts of 1983 to anable the Corporation to construct a Semiconductor Building for the proposed Integrated Circuit Fabrication Facility.

5.4.4.1 Maintenance Appropriations

Based upon the allocations of operating expenses of the Center to the State, contained in Table 5.4.3.1, the following maintenance appropriation requests are made by the Corporation in support of the Center:

Fiscal Year 1987	206,250
Fiscal Year 1988	2,753,275
Fiscal Year 1988	4,334,750
Fiscal Year 1990	4,334,750
Fiscal Year 1991	4,334,750

5.5 Benefits of the Center

Section 6(a)(4) of Chapter 40J provides that a detailed plan for a center must include a "description of the public benefits to be engendered by the center, including particularly an analysis of increased and enhanced employment and educational opportunities." The Massachusetts Microelectronics Center is intended to strengthen the educational resources of the Commonwealth and thereby increase both the attractiveness of the State as a location for economic development and expansion and the number of rewarding employment opportunities available to the citizens of Massachusetts. The beneficiaries of the creation and operation of the Massachusetts Microelectronics Center are the participating universities, particularly their students and faculty, the technology-based industries of the Massachusetts and the government and taxpayers of the Commonwealth of Massachusetts. The benefits anticipated to inure to the foregoing parties from the creation and operation of the Massachusetts Microelectronics Center as described in the First and Second Detailed Plans are recited briefly below.

5.5.1 Participating Universities

The most immediate beneficiaries of the Center are the participating universities of Massachusetts. These institutions will gain access to equipment, facilities and technical resources which they presently can not afford. This access will support

university instructional programs, faculty recruitment and development and basic and applied research programs.

5.5.1.1 Students:

- a comprehensive learning environment not now available in semiconductor and microelectronic technologies;

- access to state-of-the-art dedicated design hardware and software;

- the unique opportunity to test and electrically characterize circuits of their own design within a reasonable time after design;

- new and exciting research opportunities;

- educational opportunities in preparation for further formal education or immediate employment.

5.4.1.2 Faculty:

- access to the scientific equipment and fabrication capacity required to provide comprehensive educational experiences in semiconductor and microelectronics technologies;

- closer working relationships with industry with respect to effective curricula development and faculty research projects;

- access to Center sponsored training programs, conferences and symposia;

- access to the equipment, facilities and technical resources required for advanced research;

- opportunity to participate in an unique consortium for professional development and the recruitment of qualified graduate students.

5.4.2 Industry

The greatest benefit to industry from the Center will be a significant increase in graduating students available for employment, at all degree levels, with a comprehensive exposure to microelectronics and semiconductor technologies. Additional benefits include;

- increase in sophisticated continuing education opportunities for employees;

- exposure of a broader spectrum of university

students (e.g. physics, chemistry and materials science students) to microelectronics technologies;

- access to the Center's facilities for research on problems of interest to industry;

- availability of beta site capability for new industry equipment.

5.5.3 The Commonwealth of Massachusetts

The government and taxpayers of the Commonwealth of Massachusetts benefit substantially from the Center by maintaining the pre-eminence of the engineering universities of Massachusetts in a critical area of science and technology education, thereby supporting a strong and expanding technology-based economy in the state. The Commonwealth further benefits from the substantial private industry investment in the Center which affords a significant savings to the taxpayers of Massachusetts.

6.0 Statutory Compliance

6.1 Findings of Facts

On June 18, 1986, at its Sixteenth Meeting, the Board of Directors formally adopted the Second Detailed Plan for the Center. The Board made the first three of the following findings of fact, which were subsequently incorporated in the minutes of that Meeting. The Board delegated to the Executive Committee the authority to make the fourth and final factual finding. The Executive Committee made the fourth finding at its Twenty-Second Meeting on July 22, 1986. These findings apply specifically to the Fabrication Facility as proposed in the Second Detailed Plan:

FINDINGS OF FACT

(1) the Center as proposed in the Plan will substantially further the basic purpose of this Chapter to provide for the establishment and operation of centers for the education of qualified persons in a developing technology offering substantial employment opportunities in the Commonwealth;

(2) there is no reasonable expectation that the center as proposed in the Plan will duplicate the actual or proposed facilities or programs of a post-secondary educational institution or consortium of such

institutions located within the Commonwealth, or, to the extent that a possibility for such duplication may be found to exist, the Center as proposed in the Plan may reasonably be characterized as enhancing or supplementing the ability of such an institution or consortium of institutions to conduct such actual or proposed facilities or programs;

(3) the establishment and operation of the center as proposed in the plan are beyond the financial means of any single post-secondary educational institution or consortium of such institutions located in the Commonwealth, either because the capital costs or operating costs associated therewith are prohibitive or because the capital costs or operating costs associated with maintaining such a center at a level consistent with developing technology are prohibitive; and

(4) the Corporation has received appropriate commitments from participating businesses and participating institutions to support the center and to maintain a continuing effort to support the center; provided, that the commitments from participating businesses for project costs and start-up expenses are for support support which, in the aggregate, is equivalent in value to the amount of the proposed disbursement from the center fund and which support includes provision of the

equipment and machinery necessary and appropriate to establish the center as provided in the plan; provided, further, that the Corporation shall maintain a continuing effort to secure from participating businesses the contribution commitments required to ensure that the center is maintained at a level consistent with developing technology; provided, further, that the Corporation shall maintain a continuing effort to secure commitments from both participating businesses and participating institutions to provide qualified individuals from the employees thereof to serve from time to time as instructors at the center; provided, further, that the contributions of equipment, machinery, instructors and support of any other kind by participating businesses and participating institutions shall be at no charge to the corporation and are included in satisfaction of the requirements of the enabling act.

The foregoing findings of fact are required by Section 6(b) of Chapter 40J of the Massachusetts General Laws.

6.2 Contribution Commitments

The Board of Directors of the Massachusetts Technology Park Corporation has determined that the Corporation has received the following "appropriate commitments" to date from industry in support of the creation and operation of the Massachusetts Microeletronics Center. The value accorded these contribution commitments has been determined by the Executive Director of the Corporation pursuant to Section 6(b)(4) of Chapter 40J of the Massachusetts General Laws.

INDUSTRY CONTRIBUTION COMMITMENTS

1.) Capital (Equipment and Machinery)

CORPORATE DONATIONS	TOWARD MATCH	TOWARD PROJECT COSTS
Analog Devices *	225,000	225,000
Cameo Systems	385,000	385,000
Canon	700,000	700,000
Data General	1,275,000	1,275,000
Digital Equipment Corporation	5,141,000	4,941,000
Drytek	650,000	650,000
E G & G	50,000	50,000
FSI Corporation	411,050	411,050
Hewlett Packard	113,434	0
Inficon	12,900	12,900

Ionic	400,000	150,000
KTI Chemicals Incorporated	14,000	14,000
LAM Research	300,000	300,000
Materials Research Corporation	250,000	250,000
MTI	360,000	360,000
Northern Telecom	75,000	0
Plasma Therm	90,000	90,000
Polaroid **	300,000	300,000
Prime	3,609,000	3,609,000
PWS	35,000	35,000
Raytheon	300,000	300,000
Varian	2,712,000	845,000
VLSI Technology Inc.	3,935,000	3,935,000
	21,343,384	18,837,950

2.) Operating Contributions

Donor	FMV
- VLSI Technologies	
FY 86	$ 95,000
FY 87	$222,500
FY 88	$335,500
FY 89	$279,500
FY 90	$279,500
TOTAL	$ 1,212M

MATERIALS RESEARCH CORPORATION

Orangeburg, New York 10962 • 914 359-4200 • "Cable MATRESCO"

November 19, 1985

Dr. Joseph Stach, Executive Director
Massachusetts Technology Park Corporation
12 New England Executive Park
Burlington, MA 01803

Dear Dr. Stach:

Materials Research Corporation (MRC) is delighted to contribute the items of scientific equipment, machinery or related materials described below to the Massachusetts Technology Park Corporation (the Corporation) for inclusion in the proposed Massachusetts Microelectronics Center in Westborough, Massachusetts.

The items contributed have an aggregate fair market value of $250,000 for the sputtering equipment and $25,000 for sputtering targets. They will be delivered to the Corporation at a date to be mutually determined by the Corporation and MRC.

It is recognized that the Corporation is a public instrumentality of the Commonwealth of Massachusetts which has received a private letter ruling from the Internal Revenue Service, PLR8342022, attesting to its status as a proper recipient of deductible charitable contributions under the provisions of Internal Revenue Code Section 170(a)(1).

The specific items of scientific equipment, machinery or related materials to be contributed to the Corporation are as follows:

1) Model 203 Sputter System with an approximate fair market value of $250,000.

2) Up to seven sputtering targets specifically for the Model 203 of such materials as aluminum alloys, titanium tungsten, and silicides, or equivalent, with an approximate fair market value of up to $25,000; precious metal targets <u>cannot</u> be contributed due to the intrinsic price of the metal.

For the purpose of this correspondence, the phrase "or equivalent" represents the intention of Materials Research Corporation to provide the Corporation with the equivalent version of the above referenced items of contribution available as of the date of delivery, as agreed to by MRC and the Corporation at that time.

Any questions concerning this contribution commitment should be directed to Ross Stander.

Sincerely,

MATERIALS RESEARCH CORPORATION

Ross Stander
Director of Marketing

Sheldon Weinig
Chairman

RS/wlm

LAM RESEARCH
47655 Warm Springs Blvd.
Fremont, CA 94539
(415) 659-0200

17 JUN 85 11:

June 13, 1985

Dr. Joseph Stach
Massachusetts Technology
Park Corporation
Massachusetts Microelectronics Center
P.O. Box 663
Westborough, MA 01581

Dear Dr. Stach:

As indicated in a letter to you in May, we have committed to contribute a plasma etcher to the Massachusetts Technology Park Corporation for the Massachusetts Microelectronics Center sometime during or prior to the fourth calender quarter of 1986. In order to facilitate your planning, the approximate fair market value of the etcher to be provided will be $300,000.

If you have any questions regarding this matter, please feel free to call.

Sincerely,

Leo C. Manson Jr.

Leo C. Manson, Jr.
Treasurer

LCM:mt

cc: R. Emerick
N. Jones
T. Nicoletti
B. Surber

drytek

RECEIVED MAR 1 2 1986

March 3, 1986

Dr. Joseph Stach
Executive Director
MASSACHUSETTS TECHNOLOGY PARK CORPORATION
Massachusetts Microelectronics Center
P. O. Box 663
112 Turnpike Road
Westborough, MA 01581

Dear Joe,

Sorry for the delay in getting our written commitment to provide the MTPC with the most advanced RIE plasma etcher in the world **"THE QUAD"**.

We have four models available and it is my feeling that our **QUAD 484** will provide the greatest versatility to your organization. You can select reactors for:

1) Poly, Nitride, Silicides, etc.;
2) Oxide;
3) Aluminum Metal.

We will plan to have such a system ready for shipment the end of 1987 consistent with your facility completion date.

I have attached product literature of the **QUAD** Series for your review.

Projecting the selling price at the end of 1987, we estimate the basic **QUAD 484s** with two poly reactors, one oxide reactor and one metal reactor to be about $650,000. The actual amount we will use for tax purpose, will be determined at the time of shipment.

Sincerely,

Arthur W. Zafiropoulo
President
DRYTEK

AWZ/lrc

Enclosures

16 JONSPIN ROAD • WILMINGTON, MASSACHUSETTS 01887 • (617) 657-3933
FAX: (617) 657-8536 TLX: 272771

drytek

March 3, 1986

Dr. Joseph Stach
MASSACHUSETTS TECHNOLOGY PARK CORPORATION
Massachusetts Microelectronics Center
P. O. Box 663
112 Turnpike Road
Westborough, MA 01581

Dear Joe,

This letter serves to establish the commitment of DRYTEK INC. to contribute a Model QUAD 484s to the Massachusetts Technology Park Corporation for the Massachusetts Microelectronics Center.

As we discussed, the expected date for delivery is the fourth calendar quarter of 1987.

Sincerely,

Arthur W. Zafiropoulo
President
DRYTEK

AWZ/lrc

16 JONSPIN ROAD • WILMINGTON, MASSACHUSETTS 01887 • (617) 657-3933
FAX: (617) 657-8536 TLX: 272771

KTI CHEMICALS INCORPORATED

CORPORATE OFFICES

1170 Sonora Court, Sunnyvale, CA 94086, (408) 733-3500, TELEX 296619

85 10:

LETTER OF CONTRIBUTION COMMITMENT

May 16, 1985

Dr. Joseph Stach
Executive Director
Massachusetts Technology
Park Corporation
12 New England Executive Park
Burlington, MA 01803

Dear Dr. Stach:

Please be advised that KTI Chemicals Incorporated, a subsidiary of Union Carbide Corporation (the "Company"), has determined to contribute the items of scientific equipment, machinery or related materials referenced below to the Massachusetts Technology Park Corporation (the "Corporation") for inclusion in the proposed Massachusetts Microelectronics Center in Westborough, Massachusetts.

It is recognized that the Corporation is a public instrumentality of the Commonwealth of Massachusetts which has received a private letter of ruling from the Internal Revenue Service, PLR8432022 attesting to its status as a proper recipient of deductible charitable contributions under the provision of Internal Revenue Code Section 170(a)(1).

The specific items of scientific equipment, machinery, or related materials to be contributed to the Corporation are as follows:

1) The complete line of KTI process chemicals, including photoresists, developers, solvents, etchants, strippers, and protective coatings will be supplied at a special discount. The discount percentage will vary according to product, but no product will be sold below KTI cost. The discount amount below fair market value for the chemical products will be applied to the total contribution value. Certain new KTI products, detailed in item 2, are exempted from this discount provision.

REGIONAL OFFICES

1170 Sonora Court, Sunnyvale, CA 94086, (408) 733-3500 / 1200 West Jackson Road, Carrollton, TX 75006, (214) 245-5541
2125 West 7th Street, Tempe, AZ 85281, (602) 968-9212 / 2 Barnes Industrial Park Road, Wallingford, CT 06492, (203) 265-9242

2) Certain KTI proprietary products will be provided free of charge. At this time, this product list includes the following:

KTI Positive Photoresist 9000
KTI Positive Photoresist 9010
KTI Positive Photoresist 9500
KTI Positive Photoresist Developer SB-351
KTI Positive Photoresist Developer KMB

This list may be added to in the future.

3) KTI Chemical Dispense Units and Chemical Transport Units, or their equivalent, will be offered as contributions. The fair market value of dispense units is approximately $10,000; the fair market value of chemical transports is approximately $4,000.

For the purposes of this correspondence, the phrase "or its equivalent" represent the intention of the prospective donor to provide the Corporation with the equivalent version of the above referenced items of contribution available as of the date of delivery, as requested by the Corporation.

This contribution commitment is effective for the year 1986, and will be reviewed annually.

If you have any questions with regard to this contribution commitment do not hesitate to contact me.

Sincerely,

KTI CHEMICALS INCORPORATED

Richard L. Brewer
President

RLB:dad

cc: W. Triggs

RE.

Plasma-Therm, Inc.
ROUTE 73 • KRESSON, NJ 08053
PHONE 609 767 6610 • TELEX 83664

April 26, 1985

Dr. Joseph Stach
Massachusetts Technology Park Corporation
Massachusetts Microelectronics Center
P.O. Box 663
112 Turnpike Road
Westborough, MA 01581

Dear Joe:

This letter serves to establish the commitment of Plasma-Therm, Inc. to contribute an Inline Waf'r Stripper capable of being expanded to Nitride, Oxide and Poly to the Massachusetts Technology Park Corporation for the Massachusetts Microelectronics Center.

As we discussed, the expected date for delivery is the fourth Calendar quarter of 1986.

Sincerely yours,
Plasma-Therm, Inc.

Ronald H. Deferrari

Ronald H. Deferrari
President

RHD:js

155h

Gone
Filed from Delaware
Co. Rec
8/16/85

varian / extrion DIVISION

RECEIVED JUL 17 1985

July 15, 1985

Mr. Bill Triggs
MASSACHUSETTS MICROELECTRONICS CENTER
Massachusetts Tech. Park Corporation
P. O. Box 663
Westborough Executive Park
Westborough, Massachusetts 01581

Dear Bill:

The current list prices for the items as described in my June 5, 1985 letter are as follows:

Model 350D Ion Implanter	$ 696,460.
Spare Parts for Model 350D	19,170.
Extended First Year Warranty Service for Model 350D	15,400.
Model IA-200 Rapid Thermal Processor	99,000.
Spare Parts for Model IA-200	8,000.
Extended first year warranty for Model IA-200	7,200.
	$ 845,230.

Best regards,

Alan Schwartz

Alan H. Schwartz
Manager, Strategic Planning

AHS/ejn

c: S. Gray
M. Spelman

varian/extrion DIVISION

14 JUN 85 9:48

June 5, 1985

Mr. Bill Triggs
MASSACHUSETTS MICROELECTRONICS CENTER
Massachusetts Tech. Park Corporation
P. O. Box 663
Westborough Executive Park
Westborough, Massachusetts 01581

Dear Bill:

I am pleased that we have mutual interest in the promotion of Ion Implantation and Rapid Thermal Processing technology. In order to aid in the development of these technologies, Varian Associates/Extrion Division is prepared to provide equipment to the Massachusetts Microelectronics Center (M^2C) at no charge. I believe this equipment and the close relationship between our organizations that will be fostered during it's use will be synergistic to both parties. Please review the proposed terms of our donation which are listed below:

1. Varian/Extrion will donate a Model 350D Ion Implanter and a Model IA-200 Rapid Thermal Processor as described on Attachment A.

2. M^2C agrees to provide two qualified technicians to attend a service training program on the equipment. Varian will cover the training course expenses. M^2C will pay all costs of the techicians (salary, travel, living, etc.).

3. Varian will provide replacement parts and service which, in it's opinion, are required within the first year of operation. M^2C will pay the cost of consumables and also will pay for the costs of any replacement parts or service to maintian or repair the instrument after the first year.

4. Reasonable care must be used by M^2C to avoid any hazards. Varian/Extrion disclaims any responsibility of loss or damage caused by use of the Model 350D or the Model IA-200 other than in accordance with proper operating procedures. In no event shall Varian/Extrion be liable for incidental, consequential or special loss damage, howsoever caused.

5. Varian makes no warrantees or representations whatsoever regarding the equipment. It's merchantability, safety in operation, compliance with Federal, State or Local codes, regulations, laws, or it's fitness for any use, and M^2C expressly waives for itself and all those claiming through it any and all claims or rights against Varian which now or hereafter may arise out of the equipment or its operation or use including, without limitation, all rights of subrogation which M^2C or any insurer of M^2C may have against Varian. M^2C agrees to defend, indemnify and hold Varian harmless from all claims whatsoever arising out of the equipment or its operation or use after it's delivery to M^2C in accordance herewith.

If all the foregoing is acceptable to you, kindly indicate your acceptance by signing and dating the enclosed copy of this letter in the space provided and return the signed copy to me. I will make the necessary arrangements here.

Best regards,

Alan H. Schwartz
Manager, Strategic Planning

AHS/ejn

c: L. Hansen
R. Holzel
S. Gray
M. Spelman
J. Tompkins

Accepted by: _____

Title: _____

Date: _____

APPENDIX A

ITEM	PART NUMBER

1) Model 350D Serial Process Ion Implanter including:

A. Maximum Scanned Beam Currents of:

^{75}As	1500uA
^{31}P	1500uA
^{11}B	600uA

B. VLSI Wafer Handling System

- Throughputs of up to 350 wafers/hour
- Dual End Stations with Independent Vertical Wafer Handling Systems.
- 100 Wafer Load
- 2" - 150mm Wafer Size Compatability (One size for each end station is std.); system configured as 150mm, both end stations

C. Dose Processor - A microprocessor controlled dose monitoring system.

D. 4.3 MeV AMU Analyzing Magnet

E. XCB-80 Crystal Scan Controller - to eliminate operator set-up errors.

F. Beam Monitor Oscilloscope

G. Four Toxic Gas System

H. VHS6 Diffusion Pumps (1 each Beamline and End Station)

I. Integral Laminar Flow System

J. Spare Gas Ion Source

K. Graphite Beamline Components

L. Training and Materials for two engineers.

ITEM	PART NUMBER
Automation Options	
Remote Console, Single Bay	
Process Control Terminal (PCT)	
End Station Options	
Electron Flood Gun, both end stations	H1139001
Uniformity Monitor	H4152001
Wafer Flat Orientation, both end stations	H0317001
Hycool Wafer Cooling System (150mm)	
Additional 150mm Hycool platen	
Particulates Control Package	
Pumping Options	
CTI Cryotorr Cryopumps (beamline and end station)	H1501001
Terminal Options	
AMU Meter	09391001
Beam Energy Probe	F4881001
Electrostatic Beam Filter	F5554002
Variable Extraction	F5640001
Vaporizer Kit	08845001
Spares	
Machine spares	H0808001
"o" ring kit	H0807001
PCB spares	H0806001
Source spares	F5417001
VLSI End Station Spares	H1506001
Extended First Year Warranty	

2) IA-200 Rapid Thermal Processor including:

- Process chamber, graphite heater and power supply

- 4" Diffusion pumped vacuum system

- Wayflow^{tm} Cassette-to-Cassette End Station and Controls. (End Station equipped for one of the following wafer sizes: 3", 3-1/4", 100mm, 125mm. (Specify size at time of order.)

- IR Temperature Monitor and Wafer End-Point Temperature Controls.

- Integral Control Console with Main Control, Vacuum Control, TC Control, Process Control Panel, Anneal Cycle Control Panel, and Facilities Service Control Panel.

- Installation Supervision

- Two (2) sets of Operation and Service Manuals

- Recommended Spare Parts Kit

- Extended First Year Warranty

MACHINE TECHNOLOGY, INC.
20 LESLIE COURT
WHIPPANY, NJ 07981
(201) 386-0600 Telex: 136349

WE KEEP IT SIMPLE.

May 3, 1985

Dr. Joseph Stach
Massachusetts Technology Park Corporation
Massachusetts Microelectronics Center
P.O. Box 663
112 Turnpike Road
Westborough, MA 01581

Dear Joe:

It was a pleasure to meet with you and discuss the Massachusetts Microelectronics Center project. Machine Technology is very interested and committed to participate in this exciting venture. We are interested in, both, the Semiconductor Instructional Process Laboratory concept, as well as the Integrated Circuit Fabrication Facility for application specific integrated circuits.

In this regard, Machine Technology will commit to providing a coat-develop track model for the Instructional Fabrication Laboratory. MTI will commit to donating one TargeTrack each year for the next five years. The current fair market value of each TargeTrack is $47,000.

For the Integrated Circuit Fabrication Facility which needs to interface to scanning projection aligners, such as Perkin-Elmer Model 600 or Cannon Model 500FPA or equivalent. For your needs we propose the following system for each aligner:

1 Vacuum Vapor Prime Track
1 Photoresist Water Track
2 Interface Robots
1 Develop Track

Continued

Two such complete systems should meet your requirements. The current fair market value for these two systems is $650,000 and Machine Technology will make them available to the Massachusetts Microelectronics Center for $275,000. As mentioned, your need is for these systems to be delivered in the fourth quarter of 1986 or first quarter of 1987.

Machine Technology is looking forward to participating in the Massachusetts Microelectronics Center project.

Sincerely yours,

Gary Hillman
President

GH:jf

consilium

RECEIVED JUL 19 1985

Mr. William Triggs
Semiconductor Operations Manager
Massachusetts Microelectronics Center
P.O. Box 663
Westborough Executive Park
Westborough, MA. 01581

July 17, 1985

Dear Bill:

We enjoyed meeting with Charlie and you last week. As a follow-up we are enclosing a proposal which covers your immediate needs for a WIP Tracking System as well as some of the other modules which you expressed an interest in. All prices include our 50% discount for non profit educational institutions. Also included is some information about our company, our product and customer base.

In our work, we have found that the most common failing of manufacturing systems is the inability to adapt to new or changing user requirements. Inadequate systems fall into minimal use and are soon supplanted by manual systems and personal computers. Our goal at Consilium, therefore, has been to supply our clients with the most flexible, open system possible, while maintaining full secured control.

As the semiconductor world is one of constant change, a system hardcoded around current tasks and resources might only work for six to eighteen months before needing major modification. As indirect materials become a key source of contamination, for example, an inventory system must grow beyond simple controlling masks, gases and wafers.

Consilium's approach to system design distinguishes us from the rest of the field. We studied semiconductor industry requirements for over three years before designing COMETS. Based on broad experience with many clients, we chose to:

.Use a general statictical package instead of hardcoded trend charts and histograms.

.Track any and all inventories with full traceability not limited to masks, wafers, gases.

.Support user exits from all move transactions to let users add additional proprietary analyses and edits (an open system architecture).

.Add lot level overrides on messages, specifications, and engineering data collection so custom products and experiments can be handled easily.

.Use the full capabilities of VAX/mail, DBMS, Datatrieve, Polygraphics and other utilities, instead of writing our own.

.Build a nonlot system around entities and events, with schedules and subordinate events to support real factory management, and not just equipment tracking for setups and preventive maintenance.

Any system that cannot be tailored to users' requirements will ultimately fail. A system purchased now must be able to respond to your changing environment over the next three to five years or it will become obsolete. That is why we have designed COMETS as a flexible, open and adaptable system.

We look forward to adding you to our list of satisfied COMETS users. If you have any questions or need further information, please feel free to give me a call.

Sincerely,

CONSILIUM ASSOCIATES, INC.

Mike Lindstedt
Sales Representative

ML:j

PRICE AND DELIVERY QUOTATION

Quote for COMETS modules required to support Massachusetts Microelectronics Center's requirements.

System Description	Standard Price	Discounted Price - 50%
Immediate needs		
Advanced WIP (excluding SCRIPT)	$95,000	$47,500
Other Modules		
Advanced LEC *	$65,000	$32,500
Factory Communications	$25,000	$12,500
Specifications	$45,000	$22,500
Non-Lot (tm) Tracking System	$95,000	$47,500
Inventory	$10,000	$ 5,000

* Engineering Data Analysis (RS1 or Enhansys) can be purchased separately.

Maintenance Agreement - 15% of current list price.

This quote is dependent on:

Payment due:
- 20% on contract signature
- 60% on software delivery
- 20% within thirty days

Incorporated in the price are 20 days of training and support and two copies of all appropriate documentation.

SEMITOOL

May 12, 1986

Mr. William Triggs
Massachusetts Microelectronics Center
P.O. Box 663
Westborough Executive Park
Westborough, MA 01581

Dear Bill:

Pursuant to our recent telephone conversations I wish to confirm SEMITOOL's commitment to afford the Massachusetts Microelectronics Center a 50% discount in process tools of interest to your organization.

Included in the line will be the new Spin Rinser/Dryer which is showing consistent particle removal performance. The Water Soluble Tool and Solvent Tool continue to find a substantial market and to offer superior performance and uptime. Finally, the Spray Acid Tool will be shown at Semicon West with our new aspirated, on-demand mixing of SC-1 and SC-2, 5-1-1 processes.

In recent months SEMITOOL has been recognized as offering the first SECS-II, RS232 controlled wet-process equipment. Both in Montana and in IBM, Burlington we have operating installations today on SAT's.

Also at the show will be the SEMITHERM VTP described in the enclosed releases.

I look forward to demonstrating our capabilities further when we meet at and after the show.

Best regards,

Norman H. Lowe

NHL/kb

Enclosures

155t

(603) 622-1214 / 169 SOUTH RIVER ROAD / BEDFORD, NEW HAMPSHIRE 03102
FAX NO. (603) 623-2756

CORPORATE OFFICE
(406) 752-2107 / BOX 2169 / 655 WEST RESERVE DRIVE / KALISPELL, MONTANA 59901
FAX NO. (406) 752-5522

BTU Engineering Corporation
Bruce Systems

Esquire Road
North Billerica, MA 01862-2596 USA
Tel. (617) 667-4111, Telex 94 74
Facsimile (617) 667 9068

January 31, 1986

Massachusetts Microelectronics Center
Post Office Box 663
Westborough Executive Park
Westborough, MA 01581

ATTN: Mr. Joseph Stach

Dear Joe:

After visiting with you at your facility last October and discussing our position on Quotation #3430, we have tried unsucessfully to find a way we might modify, or augment, our proposal to make it more favorable to M^2C.

As you well know, the semiconductor business climate has not been, is not now, and does not promise in the immediate future to be conducive to generating profit. Thus, all of us involved are hanging in hoping for a business uptick. While I occasionally see an optomistic report it is where someone has searched out an escoteric indicator, I don't, as yet, see a viable or meaningful upturn and moreover, our capital equipment business lags such an upturn when it does occur. Accordingly, Joe, we are hard pressed to go beyond our offer made last October, which I still feel is generous.

In summary, the offer is: The equipment requested by M^2C was quoted May 3, 1985 at $1,431,893.00 (BTU Quotation #3430). We agreed, at that time, to donate $110,000 in software and $60,000 in spare parts making M^2C's price $1,261,893 for the package. After further discussions with you, we agreed to reduce M^2C's price for the package to $1,130,000. This we reported to you in October of last year. In other words, 21% off list at that time.

Joe, you are experienced in the business and aware of the limited profit margin on mature products such as the diffusion equipment specified, so I'm certain you can easily estimate the impact of the 21% discount on BTU. We have had price increases since this quote was made, and while the quote has expired, we will of course, honor it for the short term. We do ask that your decision to procede be made soon, as we can not keep the quotation open without limit.

We at BTU are acutely aware of the positive impact M^2C will have on the semiconductor industry in Massachusetts, and we are most anxious to support you. We also enjoy the excellent rapport we believe we have with you and Bill Triggs. There are many many reasons we want to maximize our contribution to your activity, and accordingly have done a great deal of soul searching on this matter.

Please keep us informed of your progress, and as stated above, we are sincerely interested in your success. All of us here wish you the best for the New Year. Lets hope business picks up.

Best regards,

BTU ENGINEERING CORPORATION

John H. Fabricius

John H. Fabricius
Vice President

JHF/lp

August 5, 1985

Massachusetts Technology Park Corp.
P. O. Box 663
Westborough, MA 01581
Attn: Mr. William Triggs

Ref: Quotation 12098

Dear Bill,

Per our conversation, enclosed is the quote on a Microscan system for measuring centerpoint thickness, total thickness variation, flatness - both global and site, bow/warp, centerpoint resistivity, and secondary flat location (SFL).

Included are 2 sender and 2 receiver elevators. The system will accept up to 4 receivers. You can plug one sender into the receiver section to create 1 send/3 receive at any time. You can also order extra elevators for expansion when needed.

The resistivity station accepts either the high or low range assemblies which can be interchanged by your personnel.

The price includes installation and introductory training at MTPC by ADE personnel. We also run periodic one week service/operation training programs at ADE at no charge to our customers.

We have separated the charge and no charge items with list prices shown for each so you can properly show the ADE contribution to MTPC:

Charge Item	$ 69,170.00
ADE Contributed Items	63,975.00
Total Value	$133,145.00

Please call if any questions arise.

Best regards,

Winthrop A. Baylies,
Vice President

WAB/sml

Enclosure

CC: R. H. Patriquin
R. C. Abbe

ADE Corporation
77 Rowe Street
Newton, Massachusetts 02166
Tel (617) 969-0600 Telex 922415

OUR QUOTE NUMBER	DATE
12098	7/31/
CUSTOMER R.F.Q.	DATE
VERBAL [ ] WRITTEN [ ]	

QUOTATION

PLEASE DIRECT QUESTIONS REGARDING THIS QUOTATION TO:

NAME ROBERT H. PATRIQUIN

TITLE NORTHEAST REGIONAL MAN

TO

MASSACHUSETTS TECHNOLOGY PARK CORP.
P. O. BOX 663
WESTBOROUGH, MA 01581

ENCLOSURES MICROSCAN BROCHURE
COVER LETTER

ATTENTION MR. WILLIAM TRIGGS

97

DELIVERY ITEM NO	ESTIMATED SHIPPING DATE A.R.O.	YOUR LOCAL REPRESENTATIVE	ITEM
1-15	22-24 WEEKS	ADE CORP./R. PATRIQUIN 1S REGION 97/01	1-15 1-

ITEM	QUANT	MODEL OR PART NUMBER	DESCRIPTION	UNIT PRICE	AMOUNT
1	1	8100-14	LONG FRAME BASE SYSTEM STATION 1 - WILL ACCEPT UP TO TWO SEND ELEVATORS STATION 2 - PREALIGNER STATION (WITH NOTCH, SFL OPTION) STATION 3 - FLATNESS/THICKNESS STATION STATION 4 - WILL ACCEPT ONE OPTIONAL RESISTIVITY STATION STATION 5 - WILL ACCEPT UP TO TWO RECEIVE ELEVATORS STATION 6 - WILL ACCEPT UP TO TWO RECEIVE ELEVATORS CABLE, RS232 FOR HP COMPUTER ONE DOCUMENTATION PACKAGE INSTALLATION SIX MONTHS WARRANTY AFTER ACCEPTANCE	$ 69,170.00	$ 69,170.
2	1		SYSTEM CONTROLLER AND SOFTWARE HP 9817H COMPUTER SYSTEM 1 MBYTE RAM PASCAL LICENSE DISKETTES (BOX OF 10)	9,130.00	N/C
3	1	8100-22	DUAL 3 ½" FLEXIBLE DISC DRIVE - HP 9121D	1,045.00	N/C
4	1	8100-16	SUPPLY FOR INPUT 90-130V, 60 HZ	N/C	N/C
5	2	8100-31	SINGLE SEND ELEVATOR 2 @ $4,000./EA.	8,000.00	N/C
6	2	8100-32	SINGLE RECEIVE ELEVATOR 2 @ $4,000./EA.	8,000.00	N/C
				TOTAL	

-SEE PAGE 2-

155x

TERMS AND CONDITIONS:

1. All shipments F.O.B. our plant, Newton, Mass. Payment net 30 days. Late payments are subject to a service charge of 1½% per month (18% per year) to the extent permitted by law.
2. This Quotation is valid for 30 days from date hereof after which ADE Corporation reserves the right to change it in any and all respects. Clerical errors subject to correction at all times.

SIGNATURE

ADE Corporation
77 Rowe Street
Newton, Massachusetts 02166
Tel (617) 969 0600 Telex 922415

OUR QUOTE NUMBER	DATE
12098	
CUSTOMER R F Q VERBAL ( ) WRITTEN ( )	DATE

QUOTATION

PLEASE DIRECT QUESTIONS REGARDING THIS QUOTATION TO

NAME _____

TITLE _____

TO

MASS. TECH. PARK CORP.

ENCLOSURES

ATTENTION

DELIVERY ITEM NO	ESTIMATED SHIPPING DATE A.R.O	YOUR LOCAL REPRESENTATIVE REGION	ITEM

ITEM	QUANT	MODEL OR PART NUMBER	DESCRIPTION	UNIT PRICE	AMOUNT
7	1	8100-91	SITE FLATNESS OPTION	$ 10,000.00	N/C
8	1	8100-92	BOW AND WARP OPTION	3,000.00	N/C
9	1	8100-45	TYPE OPTION (.1 - 99.9 OHM-CM)	2,000.00	N/C
10	1	8100-52	LOW RANGE RESISTIVITY STATION .001 - .99 OHM-CM AVAILABLE ON 8100-14 ONLY	7,250.00	N/C
11	1	8100-54	HIGH RANGE RESISTIVITY STATION .100 - 99.9 OHM-CM AVAILABLE ON 8100-14 ONLY	7,250.00	N/C
			CALIBRATION MASTERS		
12	1	7800-58	LOW RANGE RESISTIVITY MASTERS .001 - .99 OHM-CM, 4 PIECES, 2" DIAMETER, (.003, .009, .03, .09 OHM-CM NOMINAL)	1,100.00	N/C
13	1	7800-59	HIGH RANGE RESISTIVITY MASTERS .100 - 99.9 OHM-CM, 6 PIECES, 2" DIAMETER (.3, .9, 3, 9, 30, 90 OHM-CM NOMINAL)	1,700.00	N/C
14	1	7800-110	THERMAL PRINTER HP 2671G WITH HP 10833B	2,500.00	N/C
15	LOT		SIX MONTH SERVICE CONTRACT	3,000.00	N/C
				TOTAL	$ 69,170.0

TERMS AND CONDITIONS:

1. All shipments F.O.B. our plant, Newton, Mass. Payment net 30 days. Late payments are subject to a service charge of 1½% per month (18% per year) to the extent permitted by law.
2. This Quotation is valid for 30 days from date hereof after which ADE Corporation reserves the right to change it in any and all respects. Clerical errors subject to correction at all times.

SIGNATURE

7.0 Conclusion

The creation and operation of the Massachusetts Microeletronics Center are predicated upon the finding of the Legislature and the Corporation's Board of Directors that the strengths of our institutions of higher education are critically important for an expanding, technology-based economy for the Commonwealth. The purpose of the Center is to retain, and to a certain extent to regain, the pre-eminent position of our institutions of higher learning in the field semiconductor and microelectronic technologies. The Center is intended to strengthen the educational resources of the Commonwealth and thereby increase both the attractiveness of the State as a location for industry development and expansion and the number of rewarding employment opportunities available to the citizens of Massachusetts.

The Massachusetts Microelectronics Center as proposed in this Second Detailed Plan is a most worthwhile investment for the Commonwealth of Massachusetts. It presents the opportunity for the continued development of an unprecedented negotiated partnership among State government, industry and the engineering colleges and universities of the Commonwealth. It will provide the engineering students of the Commonwealth with a desperately needed laboratory experience in a critical area of science and technology education.

Advances and applications of semiconductor and microelectronic technologies are the basis for the economic resurgence of Massachusetts. It is no coincidence that this explosion of technology-based economic activity has occurred in a State with a wealth of institutions of higher learning. But if we are to reap the benefits of the strengths of our many academic institutions we must likewise recognize the burdens placed on these same institutions by rapidly evolving technology. The First Phase of the Center project has and will provide these institutions with the basic computational and processing laboratory equipment required for innovative instructional and research programs. And it is the intention of the Center's Board of Directors to work closely with our universities, Massachusetts industry and State government over the coming years to augment and amplify the substantial progress of that First Phase. But an important element of the Center remains to be initiated: a captive integrated circuit fabrication facility.

Without a dedicated capacity to manufacture student-designed circuits in a real time manner, no student in Massachusetts will have the opportunity for a legitimate laboratory experience in semiconductor design. This is not a minor matter. A real time laboratory experience is the defining element of each and every engineering undergraduate and graduate program, and comprehensive electrical and computer engineering programs are critical to our economy.

The key to sustained economic progress and the expansion of employment opportunities in Massachusetts is the continued expansion of existing enterprises and the development of new industries. In a technology based economy such as is characteristic of the Commonwealth, economic progress depends particularly upon the ability of our institutions of higher education to produce highly educated and skilled workers. The Massachusetts Microelectronics Center, which is to support a dramatic expansion in the provision of semiconductor instructional programs by our colleges and universities, will benefit the Commonwealth by supporting technology based industrial expansion within the borders of Massachusetts. Industry will be provided access to the educated labor pool necessary for growth and expansion. Our citizens shall be provided with the educational opportunities necessary for new and rewarding opportunities and career advancement. The net result to the Commonwealth from the creation and operation of the Massachusetts Microelectronics Center is to be the opportunity to increase the tax base, to avoid increased welfare and employment cost and to further the general welfare of the Commonwealth.

8.0 Appendices

8.1 Facility Design Information

WAGNER ASSOCIATES, INC. engineers•architects
201 Schuylkill Avenue•P.O Box 298•Reading, Pennsylvania 19603•(215) 376-8451

May 6, 1986

Massachusetts Technology Park
Corporation
P. O. Box 663
Westborough Executive Park
Westborough, MA 01581

Gentlemen:

The design of the Integrated Circuit Fabrication Facility (ICFF) in Westborough, Massachusetts is proceeding on schedule. This report presents the results of the design development phase.

Reference is made to the Revised Schematic Design Submission, dated January 15, 1986, for a description of the project, preliminary design concepts, cost estimates, and schematic drawings. We have attempted not to repeat this information in this report, but to present concepts developed as a result of design development. The report is presented in the following sections:

- Design Development
- Schedule
- Cost Estimate/Value Engineering

Appendices bound hereto include:

- Updated Drawing List
- Updated Specification List

Bound separately:

- Representative Calculations
- Specifications
- Drawings

READING PENNSYLVANIA•ORLANDO FLORIDA

- Cost Estimate Backup
- Meeting Notes

We trust this information will be useful.

Very truly yours,

WAGNER ASSOCIATES, INC.

W. J. O'Connell

William O'Connell, P.E.
Project Director

Martin J. Lenich

Martin J. Lenich, P.E.
Project Manager

WJO/MJL:bim

DESIGN DEVELOPMENT

A. Civil

Most of the civil work has been or will be completed under the renovation contract. Minor additions were made via change order to bring services under the road on the west side of ICFF. Even the catch basins, drainage manholes and hydrants have been purchased under Phase I and will be turned over in this phase for installation.

In summary, the work required under Phase II has been reduced to:

1. Install owner supplied catch basins, drainage manholes, and hydrants.

2. Excavate for HVAC and Process underground tanks and piping.

3. Excavate for electrical duct bank, foundations, water, fire protection, and sanitary.

4. General grading and clearing (minimal).

5. Relocate a short section of existing water main.

6. Paving and sidewalks

All systems, storm water, sanitary drainage, potable water and fire water, will be connected to existing services near the ICFF.

Architecture

The architectural concepts have not changed significantly since the schematic review. The building envelope and code analysis are the same and are detailed in the schematic report. The building interior finishes fall into three categories:

1. General Use (Offices, Labs) - University quality
2. Cleanspace - Medium quality
3. Mechanical Areas - Low quality

This approach was selected as a cost saving measure.

The gown area was revised to incorporate additional features. The new gown room layout includes the following:

1. Non-clean locker area
2. Clean entry tunnel
3. Clean gown storage
4. Gown pass through for clean/soiled gowns
5. Separate air handler
6. Benches/shelves/drinking fountain

In addition to the primary gown area, two small clean airlocks were added between the elevator and return air plenums for maintenance smocking. A small clean gown room was added to assembly as well.

Equipment access is similar to the schematic approach. Major equipment will be transported vertically from the loading dock area to upper levels via the freight elevator. A service area will be used at the second level to deliver equipment to the required clean bay. Each clean bay has a transomed double door at the east end.

Oversize equipment (which the elevator cannot handle) will be lifted via crane through an access panel at the southeast corner and transported through a "storage" room to the service aisle. Personnel move through the building via a system of stairs, corridors and elevators. This movement is free once the person is past the security gate at the main lobby. Access is restricted via card access and cyber lock type locks.

Major HVAC and support equipment is accommodated by overhead coiling doors and a temporary removable roof section. Once the axial fan systems are in place, they will not have to be removed as a unit and the roof section will be made permanent.

An E-beam area was added in the clean room. This impacted the interior wall and plenum system slightly, requiring extra details for this special case.

Office and conference areas were revised slightly to accommodate minor owner changes. Lab type spaces were added at the first level for Test, Gas Analysis, Wafer Clean, Assembly and Maintenance. A Facilities engineering office and maintenance locker area were added near the loading dock.

In general, the original building concept survived the design development phase fairly intact.

	Original Scheme 3/26/85	Intermediate Scheme 1/17/86	Final Scheme 4/28/86
First Floor Areas			
Offices	1,814	-	-
Mechanical	620	7,016	6,840
P.E. Maintenance	365	-	-
Lobby	702	472	567
Vestibule		96	96
Coats		108	96
Lockers		134	96
Stairs		127	128
Fab Support	3,630	4,439	5,690
HPM Storage	1,806	1,142	1,269
P.E. Support	10,080	9,060	10,414
Receiving	915	557	624
Scrubber	660	640	820
Mechanical	5,130	-	-
Electrical	925	-	-
Process Support	3,900	-	-
Service Elevator	240	163	150
Elevator	150	44	48
Service Yard	-	-	-
Bulk Gas Storage	-	-	-
Pryo Storage	-	-	-
Conference	-	-	-
Nursing Office	190	415	378
Health Room	180	-	-
Reception/Security	164	244	357
Waiting	164	-	-
Men	158	194	194

		Original Scheme 3/26/85	Intermediate Scheme 1/17/86	Final Scheme 4/28/86
		158	194	194
Women			850	972
Stair (N & S, 1 & 2)		1,500		
		33,451	26,002	28,933
Misc., Circulation and Wall Thickness		900	3,420	1,480
Footprint of 1st Floor*		34,350	29,420	30,413
Second Floor Areas				
Gown		1,425	426	537
First Dressing		-	241	213
Mechanical		710	321	337
Secretary		180	84	112
Office		250	137	130
Lounge		450	410	732
Men		158	155	151
Women		158	172	162
Elevator		110	44	55
Clean Corridor	1,004			
Clean Bay	5,824			
Service Area	2,196		18,250	14,070
Chase	4,513	13,537	1,674	
Egress Corridor		2,000	4,425	8,346
MU-Air Storage		6,600	163	
Service Elevator		80	238	
Elevator Equipment		-	-	-
Stair		625	140	0
Meeting		-	140	0
Interview		-	275	275
Conference #1		-	275	275
Conference #2		-	145	118
Office		-	121	118
Office		-	140	136
Office		-	72	64
Office		-	75	64
Office		-	72	64
Office		-	72	64
Office		-	1,227	1,227
Open Office		-	850	972
Stair (N & S, 1 & 2)		1,500		
			25,505	28,222

	Original Scheme 3/26/85	Intermediate Scheme 1/17/86	Final Scheme 4/28/86
Circulation and Wall Thickness	1,904	4,618	1,978
Footprint of Second Floor*	34,350	30,124	30,200
Third Floor Plan			
Mechanical	-	8,666	9,654
Service Elevator	-	163	160
Stair (N & S)	-	425	486
Footprint of Third Floor*	-	9,254	10,300
Summary			
First Level	34,350	29,420	30,413
Second Level	34,350	30,124	30,200
Third Level	9,300	9,254	10,300
TOTAL	78,000	68,798	70,913

* Footprint of floor is gross area.

C. Structure

Structural design development involved the detailing of schematic concepts. While few changes were required, the task was extensive due to the fairly complex exterior wall shapes required. Isolated foundation, composite floor, waffle slab and roof joist systems were finalized. Mechanical and electrical supports for pads, platforms, intertia bases and inserts were added. Formwork for trenches and tank tiedowns were noted. Retaining walls in the loading dock area were completed to work with the HPM spill containment system.

D. Vibration

The vibration concept from the schematic report has not been altered through design development. The "three building" approach (office, cleanroom, support) with isolation of the steel/concrete/steel independent structures, including foundations has been detailed. A few cases of isolated foundation interferences have been overcome by a combination of staggering column lines and cantilevering the waffle slab.

The addition of the E-beam will not impact structural/vibration design. The original floor specifications are suitable for the proposed E-beam installation.

Vibrating equipment isolation will be accomplished via a combination of springs, pads, inertia basis and building rigidity. Rotational speeds have been designed to avoid excessive energy input at any one frequency. Air handling system velocities have been kept below targets to insure minimal vibration and noise contribution.

Paul Oliphant of Applied Dynamics, Inc. (Vibration Consultant) has been actively involved in setting criteria for both building design and equipment isolation.

E. Heating, Ventilating and Air Conditioning (HVAC)

HVAC experienced a few changes since the schematic report, primarily the cleanroom indoor design criteria and chilled water system. Other minor changes affected the office/lab air handling system.

The original cleanroom indoor design criteria was the subject of intense scrutiny by WAI early in the project. While the change to 68 ± 1 F and 37-1/2 ± 2-1/2 % RH from 68 ± 1 F and 40 ± 2-1/2% RH is more in-line with the WAI recommendation, making the change at this stage just barely missed the category of major redesign. In examining the effect that the cumulative safety factors applied to coil, pump and chiller selection has on this change, it was apparent that there is absolutely no "fat" leftover after making the change.

A spinoff of the chilled water system analysis was the lack of economic justification in using free cooling with a ceramic cooling tower. Due to the low maintenance factor of the facility, we felt that the ceramic tower would be required if a free cooling mode was attempted. The cost premium for this was $140,000 and payback stretched beyond 7 years and, therefore, this option was eliminated.

With the addition of many minor lab spaces with constant exhaust, a hybrid of the pure VAV office system was designed. It is detailed on the General Airside Flow Diagram. Basically, the office portions are still VAV with a bypass feature to allow full flow. This full flow equals lab exhaust plus pressurization.

Control/monitoring will consist of a DDC system with a central station computer for access to all control and alarm functions via "universal type" alarms from all major equipment control panels. For example, a high pressure cutout on the chiller panel will be alarmed as "high pressure cutout", while the central station alarm will indicate "chiller alarm". This approach simplifies the system and reduces cost considerably.

The basic cleanroom air handling approach is unchanged. Return air balancing will be accomplished using "magnetic strip" filler panels. The HEPA vs. ULPA filter alternate should prove interesting since the two "qualified" suppliers had differing opinions on the economics of the change.

Finally, Alternate 4 (rated FRP ductwork vs. non-rated FRP with sprinklers) will prove to be the most complex alternate and should shed some light on the true cost of this insurance agency requirement.

F. Plumbing

Plumbing for the ICFF is fairly straightforward. There are four (4) full toilet rooms (2 men, 2 women), one (1) toilet/shower in facilities engineering, and a toilet area in the nurses room. Potable water is distributed to numerous sinks, water fountains and hose bibs. Potable hot water is generated at an electric water heater. Non-potable water is distributed to facility and process make-up water connections. Tempered eyewash/shower water is blended by mixing hot and cold potable water and recirculated continuously. Sanitary drainage is connected to the municipal sewer system. Special care has been taken to physically segregate waste treatment and sanitary drains to prevent accidental mixing. Storm water from the roof is routed via internal conductors to the storm drain system. Natural gas piping connects the boilers with the COMGas meter.

Process piping is routed in each chase overhead with stub valves for easy future connection. High purity piping mains are routed under the waffle slab with valve stubs for future extension in the chase (except nitrogen - full routing).

In general, the plumbing has changed little since the schematic presentation. All water will be metered per recently changed town water meter requirements.

Fire Protection

The sprinkler system was preliminarily reviewed with Factory Mutual and the Town of Westborough Fire Chief. The system consists of multiple zones serving nearly all areas (except electrical room and water reactive storage). Sprinklers are also provided in non-rated exhaust ductwork (alternate bid).

Seven zones are planned:

1. 1st Level - Chemical Dispense/Storage
2. 1st Level - All other areas on 1st Level
3. 2nd Level - Cleanroom Chase
4. 2nd Level - All other areas on 2nd Level
5. 3rd Level - Recirculation Air Handlers
6. Loading Dock
7. Ductwork

The loading dock is unheated and, therefore, will be a dry type system. Use of non-rated exhaust ductwork which requires sprinklers also requires drainage fittings and extra access doors.

In general, all areas will be light hazard except the cleanroom and chase area - Ordinary Hazard Group 3, 0.21 GPM/SF over 1,500 SF (sidewall heads staggered); and the Chemical Dispense/Storage Area Extra Hazard, 0.6 GPM/SF over 96 SF. The water system is connected to the Westborough water main, therefore, no on-site storage is required.

H. Process

Little changed on the process layout since there was little to change from due to the uncertainty in process equipment (a normal occurrence on a project of this type). One exception to this was the addition of an E-beam which impacted all trades, especially HVAC and Architectural.

Process Support resembled the Process in that the only impact on design development changes was brought about by the E-beam.

In general, all support systems shall be packaged, skid mounted, and prepiped and wired. This simplifies system responsibility and maintenance. All systems are located in the 1st Level mechanical support areas.

The only technical change to equipment design affects the house vacuum system which will include a wet separator and use PVC distribution piping.

Bulk gas systems will be provided by Liquid Air. The deionized water system will be bid competitively since Ionics is not offering to donate (deep discount only).

Hazardous Production Materials (HPM) will be handled as follows:

A. Deliver via truck to loading dock area. Loading dock is spill contained (no drainage) with a weather enclosure.

B. Dock leveler allows manual or forklift unloading. Spill at this point is still within containment area.

C. Delivery to storage as follows:

Pyrophorics	- Stay outside, located in cabinet along exterior wall; travel distance about 50 feet.
Flammables	- Via HPM corridor to segregated, ventilated, contained area.
Non-Flammables	- Same as Flammables

D. Delivery to dispense area as follows:

Pyrophorics	- None - dispense direct to process equipment from exterior.
Flammables	- Via HPM dispense area to point of use on 1st Level under waffle slab and process equipment

Or

Via elevator to 2nd Level to built-in cleanroom chemical closet accessible from service area.

Non-Flammables - Same as Flammables.

E. Drainage as follows:

Process waste collected via drain system and directed to waste treatment.

Other wastes not suitable for waste treatment and ultimate discharge to municipal sewer collected locally and stored in cannisters near loading dock for removal by hazardous waste contractor.

Chemical spills contained, not drained. Clean up as required.

Sprinkler flow in flammable storage areas, overflow to double wall steel tank/pipe system with leak detection. If contaminated, pump out to hazardous waste contractor; if not, pump to waste treatment.

This approach, combined with engineered controls which will be implemented in the equipment installation phase, affords the optimum in safety and cost in that it contains environmental hazards, it segregates incompatibles, it segregates hazards from personnel, it meets code requirements, and it conforms with the latest thinking in this sensitive area without being economically impractical.

I. Electrical

There were no significant changes to the electrical concept except secondary protection is now via circuit breaker instead of fuses. A number of minor systems were clarified during design development:

A. No night lighting on helicopter pad

B. Card reader with log in/out capability

C. Cameras in CAD and at ICFF

D. Lighting - cleanroom - 2 bays "yellow"

E. Gas monitoring - multipoint leak detection

F. Public address - not multibuilding

G. Telephone - Northern Telecom interface

H. Fire alarm - coordinate with renovation phase

I. Emergency generator - oil fired - 200 KW

In general, design development centered on coordinating electrical requirements with other trades for motor sizes/locations and light fixture locations.

J. Bidding

The project will be bid in accordance with Massachusetts laws governing the procurement of construction services using State funds. This requires that filed sub-bids be received for various trades. The effect that this has on the contract documents can be described as follows:

A. MTPC will award a single prime contract.

B. WAI will design a multiple prime package since each sub-bid stands alone until absorbed in A. above.

For this project, 15 filed sub-bids (or separate "prime" contracts) are required.

No.	
01	Masonry
02	Miscellaneous Steel and Metal Fabrications
03	Single-Ply Membrane Roofing and Flashing
04	Sealants/Waterproofing/Dampproofing
05	Metal Windows
06	Glass and Glazing
07	Ceramic Tile
08	Acoustical Ceiling Systems
09	Resilient Flooring
10	Painting
11	Plumbing
12	Heating, Ventilating and Air Conditioning
13	Fire Protection/Sprinklers
14	Electrical
15	Elevators

In addition to the filed sub-bid complication, five (5) alternate prices to the base bid are indicated.

1. Delete helicopter pad

2. Replace 99.9995% ULPA filters with 99.99% HEPA's

3. Delete backup power feed

4. Replace rated fiberglass exhaust duct with sprinklered, nonrated FRP duct

5. CMU in place of poured foundation walls

These items are opportunities for owner selection of options based on price. Where applicable, selection of what is base bid vs. alternate bid is designed to insure that the alternate is a deduct. This was agreed to as the proper psychological approach. The remainder of the Frontend document is similar to that use in the renovation project.

Please note that the cost estimate is categorized to match the filed sub-bids and alternates mentioned above and that the value engineering analysis will be reviewed prior to receipt of bids.

K. Permits

Numerous permits are required prior to, during, and after project construction. These are summarized below along with their current status. Many of the permits will require active follow-up, since actual equipment data is required and at this stage, due to competitive bidding requirements, we can only offer an equipment specification. This has been reviewed with the affected agencies.

	By	4/25/86 Status
EPA Storm Water	WAI	Awaiting Response
Hazardous Waste, Federal	WAI	Awaiting Response
Hazardous Waste, State	WAI	Awaiting Response
Air	WAI	Awaiting Response
Water	WAI	Awaiting Response
Pretreatment	WAI	Awaiting Response
Special Waste Discharge	WAI	Awaiting Response
Treatment Plant Connection	MTPC (Assistance by WAI)	
Sewer Connection	MTPC (Assistance by WAI)	
Water Connection	MTPC (Assistance by WAI)	
Fire System	MTPC (Assistance by WAI)	
Fire Alarm Connection	MTPC (Assistance by WAI)	
Plumbing System Review	WAI	100% Documents to be sent to DEQE
Building Inspection	Contractor	

	By	4/25/86 Status
Explosives (Storing) License	MTPC	
Fire Extinguisher Installation	Contractor	
Oil Burning Equipment Installation	Contractor	
Site Approval	MTPC/WAI	Approved
Helicopter Pad - FAA	WAI	Awaiting Response
Insurance Approval	MTPC	
Dig Safe	Contractor	
Construction Permits - Building	Contractor	
Construction Permits - HVAC	Contractor	
Construction Permits - Plumbing	Contractor	
Construction Permits - Electrical	Contractor	
Construction Permits - Municipal Sys.	Contractor	

Permitting does not appear to be a problem considering the current schedule.

8.2 Facility Construction Implementation Schedules

SCHEDULE

Final Review Meeting	5/7/86
Design Development Report Complete	5/8/86
Bid Documents Ready; Bid Advertisement	8/19/86
Receive Filed Sub-Bids	10/01/86
Receive Prime Bids	10/15/86
Award Contract	11/01/86
Start Construction	11/15/86

8.3 Board of Directors Membership

Joseph D. Alviani, Secretary
Executive Office
of Economic Affairs

Dr. L. Bryce Andersen, Dean
College of Engineering
Southeastern Mass. University

Dr. Aldo Crugnola, Dean
College of Engineering
University of Lowell

Rev. John E. Deegan
O.S.A., President, Merrimack College

Franklyn G. Jenifer, Chancellor
Board of Regents of Higher Education

Jerald G. Fishman
Group Vice President - Components
Analog Devices, Inc.

Dr. Richard H. Gallagher
Vice President & Dean of Faculty
Worcester Polytechnic Institute

Milton Greenberg
Former Chairman and CEO, GCA

Dean James E. A. John
College of Engineering, U/Mass

Dr. Russel C. Jones
Vice President for Academic Affairs
Boston University

Jeffrey C. Kalb, Vice President
Low End Systems & Technologies
Digital Equipment Corporation

George S. Kariotis, Chairman and
Chief Executive Officer,
Alpha Industries

Frank Keefe, Secretary
Admin & Finance

Stephen Kiely, Vice President
Systems, Marketing & Development
Prime Computer, Inc.

Robert C. Miller, Senior VP
Business Group, Data General

Dean Frederick C. Nelson
College of Engineering, Tufts

Michael I. Payne
V.P. for Development, SPG Corp.

Dr. Joseph F. Shea, Senior VP,
Engineering, Raytheon

Dr. Edward Simon
Vice President, Technology
Unitrode Corporation

Dr. Fred M. Tuffile
President, Sage Technology

Dr. Karl Weiss, VP Research &
Vice Provost, Northeastern

Dr. Gerald L. Wilson
Dean, School of Engineering
Mass. Institute of Technology

8.4 Biographical Sketches of Board

Joseph D. Alviani

Joseph D. Alviani was appointed Secretary of Economic Affairs by Governor Michael S. Dukakis on December 16, 1985. As the Secretary of Economic Affairs, Alviani serves as the State's chief policymaker in the areas of economic development, job training, and international trade.

Prior to his appointment by Governor Dukakis, he was a partner in the Boston law firm - Goodwin, Procter and Hoar. Mr. Alviani has a diverse background in both law and government. From 1981-1985 he was President of the New England Legal Foundation (NELF), a private non-profit economic public interest law firm.

While at NELF, he worked with government, labor and business officials to create the State's historic Right-To-Know law; which makes workplaces safer and citizens aware of toxic chemicals in their neighborhoods while protecting trade secrets.

Mr. Alviani served as Corporation Counsel for the City of Boston in 1979-80 after serving two years as Special Counsel to the mayor of Boston. He has also served as the Assistant Executive Director of the United States Conference of Mayors where he was responsible for employment and training programs. As an Associate Counsel for the U.S. House Select Committee on Labor, he drafted portions of the legislation creating the Comprehensive Employment and Training ACT (CETA). He also worked on amendments to the federal Occupational Safety and Health Administration Act (OSHA).

A Phi Beta Kappa graduate, he earned his B.A. from Dartmouth College in 1967 and a Juris Doctor in 1970 from Harvard Law School. He and his wife, Judith Fields Alviani, and their son Matthew reside in Wellesley.

As Secretary of Economic Affairs, Mr. Alviani also serves as Chairman the State's Bay State Skills Corporation. He is a member of the Board of Directors of the Massachusetts Technology Park Corporation, the Massachusetts Centers of Excellence Corporation, and the Massachusetts Student Loan Authority.

Laird Bryce Andersen

Laird Bryce Andersen was born September 16, 1928, in Madison, South Dakota. He received a B.S. in Chemical Engineering, a M.S. in Metallurgy and a M.A. in Psychology from the University of Minnesota; he received a Ph.D. in Chemical Engineering from the University of Illinois.

Dr. Andersen served as Assistant Professor at Lehigh University, Associate Professor at Rice University and the University of Nebraska, and Professor at New Jersey Institute of Technology and Southeastern Massachusetts University. He is currently Dean of the College of Engineering at Southeastern Maassachusetts University.

His academic administrative experience includes Associate Dean of Engineering, Dean of Engineering, Dean of Academic Affairs, Vice President for Academic Affairs and Acting Dean of Engineering at New Jersey Institute of Technology; and Interim Dean of Faculty at Southeastern Massachusetts University.

His industrial experience includes work at Sun Oil Company, E. I. duPont de Nemours and Company, Oak Ridge National Laboratory and Argonne National Laboratory.

Dr. Andersen's professional activities include numerous services for the American Society for Engineering Education, the American Institute of Chemical Engineers, Accreditation Board for Engineering and Technology, and the National Academy of Engineering. He is a member of the Sigma Xi, Tau Beta Pi, Phi Lambda Upsilon, Alpha Chi Sigma, Triangle honor societies, and is a licensed Professional Engineer, registered in New Jersey and Massachusetts.

Dr. Andersen's community services include participation in the Stevens-Gesner Project (New York), the Morristown Unitarian Fellowship, the First Unitarian Church of New Bedford, and member of the Board of Directors of the Massachusetts Technology Park Corporation since 1982.

Dr. Andersen is the author of two books and several articles which have been published during the years 1955-1980.

Aldo Crugnola

Aldo Crugnola is Dean of Engineering at the University of Lowell (formerly Lowell Technological Institute). Prior to this position, Professor Crugnola was Chairman of Plastics Engineering. He holds a Sc.D. in Materials Science and Engineering from the Department of Mechanical Engineering at the Massachusetts Institute of Technology. Before joining Lowell in 1968, Dr. Crugnola was an Institute Researcher at the Institute for Industrial Chemistry in Milan from 1963 to 1968 and a Research Physicist for the U.S. Army Laboratories in Natick, Massachusetts, from 1954 to 1963.

Dr. Crugnola is the author of seventy Journal articles and Technical papers in the areas of a) the Relation Between the Chemical/Physical Structure of Polymeric Materials and their Mechanical/Physical Properties; b) the effect of Processing on the Structure and Properties of Polymeric Materials; c) the Processing and Properties of Reinforced Plastics; and d) the use of Plastics in Orthopedic Surgery.

John E. Deegan

A native of Hoosick Falls, New York, Rev. John E. Deegan, O.S.A., was formally inaugurated as Merrimack College's fourth president on October 24th in the Collegiate Church of Christ the Teacher, the very same church in which Fr. Deegan took his vows as an Augustinian priest on June 3, 1961.

Father Deegan comes to Merrimack College after serving as Vice President for student life at Villanova University for five years. A member of Merrimack's Board of Trustees since 1978, he holds a Bachelor of Arts degree and Masters degrees in Modern European History and Secondary School Administration, all from Villanova. In 1971, Father Deegan received his Ph.D. in Student Personnel Administration in Higher Education from American University in Washington, D.C.

He began his teaching career in 1961 at Monsignor Bonner High School in Drexel Hill, Pennsylvania, where he also served as an Administrator until 1969 when he began working toward his Ph.D. at American University. While at American, he became active in student life and activities. He served in various positions including Administrative Intern to the Vice President for Student Life, Coordinator of Cooperative Study Program for Black and Other Minority Students, and Coordinator of Graduate Activities.

In 1972, Father Deegan was appointed Associate Dean of Student Activities and Assistant Professor of Education at Villanova University. In 1975 he served as Acting Chairman of the Department of Education and was appointed the Vice President for Student Life at Villanova in 1976.

Throughout his years as an Administrator at Villanova, he held memberships on the Environmental Committee, the University Planning Committee, the Student Life Committee, the Priorities Committee, and he was co-author of a policy statement on the goals and objectives of the university.

Father Deegan has written extensively on student relations with both faculty and administration, and he has done substantial research in values and values clarification.

In March of 1981, the Board of Trustees of Merrimack College chose Fr. Deegan as Merrimack's fourth president. He assumed his duties on June 1, 1981.

Joseph M. Finnegan

[Former Acting Chancellor, Massachusetts Board of Regents. As of the date of this writing, the Center has no biographical information regarding his successor, Dr. Franklyn G. Jenifer, the new Chancellor of the Board of Regents.] Joseph M. Finnegan is a resident of Walpole where he lives with his wife and two children. He graduated from Boston College with an A.B. in Economics and from Suffolk University with an M.B.A. in Financial Management. Mr. Finnegan also completed various courses at the Department of Education in Boston, the Dale Carnegie Institute (Boston) and New York University.

In December 1985, Mr. Finnegan was appointed to the distinguished position of Chancellor, Board of Regents - the chief executive of the public higher education system and prinicpal advocate for higher education in Massachusetts.

Prior to this position, Mr. Finnegan held the office of Vice Chancellor from July 1981. Mr. Finnegan has also served as Deputy Commissioner for Fiscal Affairs at the Executive Office for Administration and Finance, and in several capacities at the Department of Mental Health from 1966 - 1979, where he received a ten-year outstanding service award - the first employee ever to receive such an award.

Mr. Finnegan has served as a member to the Special Commission on the Status of Buildings Occupied by the Judicial Branch; is a member of Alumni Career Network, Suffolk University, providing varying degrees of assistance to students and alumni who are looking for information about careers and occupational preparation; is Vice Chairman of the Board of Directors of the Neponset Valley Health System in Norwood; is a member of the Board of Trustees at Southwood Community Hospital; and is a member of the Board of Directors of the following: The Catholic Charitable Bureau of Boston, New England Initiatives, and Health Care Laboratories, Inc.

Jerald G. Fishman

Mr. Fishman is Group Vice President-Components of Analog Devices, Inc. His responsibilities include those divisions that design, manufacture, and market monolithic and hybrid integrated circuit components. Included are the Company's two semiconductor divisions, ADS in Wilmington, Massachusetts, and ADBV in Limerick, Ireland. Also included are the Wilmington-based Microelectronics Division, and the Computer Labs Division in Burlington, Massachusetts.

Mr. Fishman joined the Company in 1971, progressed through a series of marketing positions, and was named Director, Monolithic Procducts in 1979. He was promoted to General Manager - ADS in 1979, became a Vice President in 1980, and was promoted to his present position in 1982. He also serves as the Corporation's Stragtegy Manager for Components.

Richard H. Gallagher

Dr. Gallagher was born in New York City November 17, 1927. He graduated from New York University with a B.C.E. and from Suny of Buffalo with an M.C.E. and a PH.D.

Dr. Gallagher experience to date includes work as a Field Engineer at the Department of Commerce, Jamacia, N.Y., a Structural Designer at Texaco, New York City; Assistant Chief Engineer at Bell Aerospace Co.; Professional Civil Engineer at Cornell University; Dean, College of Engineering, University of Arizona; and is currently Vice President and Dean of Faculty at Worcester Polytecnic Institute.

Dr. Gallagher is an author and editor, served in the USNR, and received the following honors: Fullbright Fellow, Austria; Science Research Council Fellow, U/Wales; and Fellow ASCE, ASME. He is a member of AIAA, and American Society of Engineers Foundation, the National Academy of Engineering, Society Experimental Stress Analysis, Sigma Xi, Chi Epsilon, and Tau Beta Pi.

Milton Greenberg

Milton Greenberg was formerly President, Chairman and Chief Executive Officer of GCA Corporation in Bedford, Massachusetts.

Previous experience includes the position of Deputy Director and Chief of Operations & Planning, Geophysics Research Directorate, Air Force Cambridge Research Center in Bedford.

Through the years, Mr. Greenberg has been very active in various government activities and technical organizations; he served in the U.S. Air Force from 1942-47.

Mr. Greenberg graduated with a B.A. in Science from the College of the City of New York and New York University; an M.S. (Equivalent), Technical School, Air Force Technical Center; an M.P.A. from Harvard University; and a Sc.D. (honorary) from both Canaan College and Merrimack College.

He is the author of articles and reports on technical subjects (many classified) and on the organization and administration of research and development activities and has published keynote addresses.

Mr. Greenberg is a member of the following honor societies and has received the following recognition: Mu Chi Sigma, Beta Lambda Sigma, Army Commendation Ribbon; Medal for Exceptional Civilian Service to the Air Force, Leaders in Electronics, Men of Achievement, Who's Who in America, Who's Who in Finance and Industry,and Who's Who in the World.

James E. A. John

James E. A. John currently holds the distinguished position of Dean, College of Engineering, University of Massachusetts. Prior to this position, which he has held since 1983, he served as Professor and Chairman, Department of Mechanical Engineering at Ohio State University and the University of Toledo. His experience also includes work at the National Academy of Sciences, Washington, DC; the University of Maryland, Department of Mechanical Engineering; the Air Reduction Company, Inc., Murray Hill, N.J.; and the University of Missouri.

Dr. John received his B.S.E. and his M.S.E. in Aeronautical Engineering from Princeton University in 1955 and 1957, respectively; and his Ph. D. in Mechanical Engineering from the University of Maryland in 1963.

Dr. John is a member of the following Professional and honor Societies: American Society of Mechanical Engineers, American Society for Engineering Education, Society of Automotive Engineers, Pi Tau Sigma, Tau Beta Pi, Sigma Xi, and Phi Kappa Phi. He received acknowledgments in: Outstanding Educators of America, American Men of Science, Who's Who in the Midwest, Who's Who in Aviation, Who's Who in Engineering, Who's Who in America, Outstanding Teacher Award, Triangle Fraternity (1976), SAE Teetor Award (1979), and Fellow - ASME (1983).

John is the author of numerous publications during the years 1978 - present and is the author of three engineering text books.

Russel C. Jones

Russell C. Jones was born in Tarentum, Pennsylvania, October 18, 1935. He was educated at the Carnegie Institute of Technology where he received his B.S.C.E., his M.S.C.E. and Ph.D in 1957, 1960, and 1963, respectively. He attended the Harvard Business School, Institute for Education Management in 1975.

Dr. Jones is currently Vice President for Academic Affairs at Boston University where he has direct line responsibility for several academic units, staff functions, and University committees. Formerly, he served as Dean, School of Engineering, University of Massachusetts; Professor and Chairman, Department of Civil Engineering, Ohio State University; and Assistant and Associate Professor of Civil Engineering at the Massachusetts Institute of Technology.

Dr. Jones is a member of several professional societies and among many honors achieved are Tau Beta Pi, Sigma Xi, Phi Kappa Phi and Chi Epsilon.

Dr. Jones has authored or co-authored at least sixty publications, is a member of many professional societies, is the recipient of numerous awards and recognition, and is a registered professional engineer - registered in Pennsylvania, Massachusetts and Ohio.

Jeffrey C. Kalb
Chairman of the Board of Directors, MTPC

At Digital Equipment Corporation, Jeffrey C. Kalb is Vice President, Low End Systems and Technology; he has been with Digital since 1981. He is responsible for the design, development and manufacturing of custom semiconductors for Digital; additionally, has the responsibility for semiconductor procurement operations amounting to over $250M in total expense, material, and capital. Mr. Kalb is a member of the corporate Management Committee, the Engineering Management Committee and the Manufacturing Staff.

Mr. Kalb has held several professional positions with Data General Corporation, National Semiconductor and Texas Instruments.

Mr. Kalb is a graduate of the University of Cincinnati where he received his B.S.E.E., Magna Cum Lauda; he was named outstanding graduate of the University of Cincinnati twelve years after graduating and is still the youngest person to hold this honor.

Mr. Kalb has written eleven magazine articles or applications notes and co-authored a book; he is actively involved in numerous civic and church organizations.

George S. Kariotis

George S. Kariotis is the founder, Chairman, and Chief Executive Officer of Alpha Industries, a major producer of microwave devices and components for defense and commercial applications.

Mr. Kariotis received his B.S. in Electrical Engineering with honors from Northeastern University in 1943 and served as a naval officer in the Pacific Theater in World War II. After the war, he worked as an engineer and, in 1949, joined the Sprague Electric Company, where he eventually became General Manager of the Pacific Division. In 1956, he returned to the Boston area as Vice President of Sales of Microwave Associates (now M/A-Com).

In 1962, Mr. Kariotis founded Alpha Industries. The Company has become one of the world's largest independent producers of microwave semiconductors and components with yearly sales in excess of $70 million. Approximately 60% of the company's sales are to the defense electronics markets; the balance consists of microwave products sold to the telecommunications industry and for commercial rader and motion detection applications.

Mr. Kariotis took a four-year leave of absence from Alpha beginning in January 1979 when he was appointed by Massachusetts Governor King to a four-year term as Secretary of Economic Affairs. While serving on the Governor's cabinet, Mr. Kariotis conceived the ideas for the Bay State Skills Corporation and the Massachusetts Technology Park Corporation. These two public/private partnerships were enacted into law, and Mr. Kariotis serves them both, first as Chairman and currently as a member of their Boards' of Directors.

Exceptionally active in educational activities, Mr. Kariotis serves on the Board of Trustees and is a member of the Corporation of Northeastern University. He has also served on various committees at Tufts University, the Sloan School of Management at MIT, the University of Massachusetts, and Merrimack College.

Mr. Kariotis also is a member of the Board of Directors of the Massachusetts High Technology Council, the Associated Industries of Massachusetts, Lahey Clinic Foundation and Dranetz Technologies, Inc.

Frank Keefe

Born in Boston, Massachusetts, and educated in pohilosophy, politics and economics at Fordham (BA) and Oxford (BA, MA) universities, Mr. Keefe started his career in 1968 as a Management Trainee and later as staff Assistant to the Director of Planning and Development at the New York Port Authority, where he worked on a wide variety of transportation projects.

Returning to Massachusetts in 1971, Mr. Keefe became the Assistant Director of the Northern Middlesex Area Planning Commission in Lowell, and became Lowell's City Planning Director in late 1973. In the spring of 1975, Mr. Keefe left Lowell to become Massachusetts' first Director of State Planning under former Governor Michael Dukakis. He remained in State government until January 1979, at which time he became President of Harrington, Keefe & Schork, Inc., a planning and development firm emphasizing private sector urban development, adaptive reuse and new development approaches and techniques.

Mr. Keefe has actively participated on many local and state committee on a voluntary basis, has researched and written several papers which were published in the seventies, and took part in the writing and/or directing of the development of numerous area development projects and/or plans.

Robert C. Miller

Mr. Miller is responsible for the overall planning, development and marketing of Data General's computer systems. Reporting to Mr. Miller are the Company's Business Group Marketing organization, System Development Division, Federal Systems Division, Distribution Division, Business Group Planning organization, and Japanese Business Development business unit. Mr. Miller reports to Edson D. de Castro, President of Data General.

Mr. Miller, 42, joined Data General as Senior Vice President of Technology in June, 1981. He became Senior Vice President of the Company's Business Divisions in August, 1982, and Senior Vice President when the Business Divisions reorganized to increase emphasis on industry marketing programs and product marketing.

Mr. Miller previously was with IBM for 15 years, where he held a number of product development and marketing management positions. He held key responsibilities in product management of the IBM 4300 Series and IBM 8100 Series as well as display, microprocessor, and semiconductor products.

Mr. Miller has a B.S. in Mechanical Engineering from Bucknell University and an M.S. from Stanford University.

Mr. Miller holds six patents, is the author of several technical articles and holds an IBM "Invention Award".

Mr. Miller is a member of the Board of Directors of the Corporation for Open Systems (COS) representing Data General which became a Senior Research Member of COS in February, 1986. He is also a Director of the Massachusetts Technology Corporation. Mr. Miller is a New York State professional engineer, a senior member of the International Association of Electrical and Electronics Engineers and a member of the National Society of Professional Engineers.

Dr. Frederick C. Nelson

Dean Nelson graduated from the Tufts College of Engineering in 1954 and received his Ph.D in applied mechanics from Harvard University in 1961. He joined the Tufts faculty in 1955. His teaching interests are in solid mechanics, acoustics, and thermodynamics. His research interests are in structural dynamics, structural damping, and machinery noise control. He has reported his research in more than 40 papers and has been a consultant to more than a dozen companies. Dr. Nelson became chairman of the Department of Mechanical Engineering in 1969, Professor of Mechanical Engineering in 1971, and Dean of the College of Engineering in 1980. He has spent one term in England as a Visiting Research Fellow at the Institute for Sound and Vibration Research, University of Southampton, and two terms in France as Visiting Professor at the Institute National des Sciences Appliquees de Lyon.

A part of Dean Nelson's teaching effort has been explaining technology and its effects to non-engineers. In this regard, he has lectured on the early development of the steam engine, the Industrial Revolution, the objective and subjective aspects of noise, and the assessment and management of risk.

Dean Nelson is a Fellow of the Acoustical Society of America, a member of the American society of Mechanical engineers, and a member of the American Association for the Advancement of Science. In 1980, he was awarded the Centennial Medallion of ASME for his application of the technologies of mechanical engineering to the solution of problems. He has four children and resides in Reading, Massachusetts.

Michael I. Payne

Mr. Payne is the Vice President of Development at SPG in Billerica MA. The Company is a "start-up" involved in mechanical CAE software. Previous to that he was the Eastern Region Manager for Phoenix Data Systems, a company that produced software for VLSI mask verification. He was previously the Director of R&D for the CAD/CAM products that Prime markets. The products are in three market segments: Electrical, Mechanical and Architectural Engineering & Construction (AEC). Prior to that he was responsible for Business Development in CAD/CAM and for 6 years he ran the Microelectronics Group within Engineering where he developed integrated circuits for a microcomputer. Mr. Payne spent 5 1/2 years at RCA Solid State where he had a variety of assignments, including managing the development of the semiconductors for the Trident missile.

Mr. Payne holds a BSEE from Southampton University, a MS in Physics from London University and a MBA from Pace University in New York. He is a member of the Board of Directors of the Massachusetts Technology Park Corporation. Mr. Payne lives in Wakefield with his wife, Frances, and their four children.

Dr. Joseph F. Shea

Dr. Shea holds B.S., M.S. and Ph.D degrees from the University of Michigan.

At Bell Telephone Laboratories, he started as Research Mathematician and in 1956 became Military Development Engineer. At General Motors from 1959 to 1962, he was Director of Advanced Development and Manager of Ballistic Missile Guidance Developments. In 1962, he joined NASA as Deputy Director of Manned Space Flight for Systems Engineering where he directed the studies which led to the selection of Lunar Orbit Rendezvous as the Apollo Mission Mode. From 1963 to 1968 he was manager of the Apollo Spacecraft Program at Houston. Dr. Shea joined Raytheon in 1968 as Vice President and General Manager of the Equipment Division and became Group Executive in 1975. In 1981 he assumed his present position as Senior Vice President, Engineering, responsible for technology and advanced planning throughout the Corporation.

A member of the National Academy of Engineering, he has been involved in many studies for the National Research Council and the Department of Defense.

Dr. Edward Simon

Dr. Edward Simon is the Vice President of Technology at Unitrode Corporation in Lexington.

Dr. Simon is a graduate of Purdue University where he received an M.S. in Theoretical Physics in 1952 and a Ph.D. in Solid State Physics in 1955.

From 1958 to 1967, Dr. Simon served as co-founder and subsequently, President, of Solid State Products, Inc., where he was responsible for the development of the first commerical signal and low power SCR, the GTO SCR, and the light-triggered SCR; silicon alloy diffused transistors; epitaxial SCR for nuclear radiation environments; silicon planar power transistors; silicon planar epitaxial transistors and SCR's; and the first commercial use of electron bombardment for lifetime control. Dr. Simon initiated his employment relationship with Unitrode Corporation in 1967, upon its merger with Solid State Products, Inc.

Dr. Simon is responsible for four patents in silicon device and process technology; he has presented papers at IEEE and ECS meetings; written several articles for company use and for popular technical journals in the area of radiation effects, detection and hardening.

He is a member of the IEEE, ECS, APS, Sigma Pi Sigma and Sigma Psi societies, and the recipient of many honors and awards as: Leaders in American Science, International Who's Who, Who's Who in the East, Who's Who in Technology Today. Dr. Simon was appointed to the Board of Directors of the Massachusetts Technology Park Corporation in November, 1982, and re-appointed by Governor Dukakis for a 5-year term in February 1984; he is presently Vice Chairman of the Executive Committee and Chairman of the Fabrication Oversight Committee. Additionally, Dr. Simon is on the Industrial Advisory Board, Department of Electrical and Computer Engineering of the University of Massachusetts, Amherst; Consultant to Computer Place, Museum of Science, where he has recently been appointed to the Board of Governors.

Fred M. Tuffile

Dr. Fred M. Tuffile is currently President of Sage Technology, a division of Polaroid. Prior to his current employment he worked for Polaroid Corporation in Waltham, Massachusetts, from 1971 through October 1985.

Dr. Tuffile received his B.S. in Chemical Engineering from the University of Detroit, his M.S. in Chemical Engineering from Rensselaer Polytechnic Institute, and his Ph.D. in Physical Chemistry from Seton Hall University.

He is professionally affiliated with the American Institute of Chemical Engineers and the American Chemical Society - Sigma XI. He is the author of Technical Publications and Patent.

Memberships have included: Board of Directors of Greater New Bedford Area Chamber of Commerce, Chairman of the Committee on State Taxation and Legislation for the Chamber, member of the 1980 Program Committee of he Massachusetts Taxpayers Foundation, Inc., Trustee of St. Luke's Hospital in New Bedford, and Director of the Massachusetts Technology Park Corporation.

Karl Weiss

Dr. Karl Weiss was born in Hamburg, Germany, and received his early education in Germany and England. A U.S. citizen since 1952, he holds a B.S. degree in chemistry from Columbia University (1951) and a Ph.D. in chemistry from New York University (1957). He started his academic career at New York University in 1956 and joined Northeastern University in 1961 where he has been Professor of Chemistry since 1965, and has served as Chairman of the Department from 1969-1979, as Vice Provost for Research and Graduate Studies from 1979-1983, and as Vice President for Research and Vice Provost since 1983. As Vice President/Vice Provost, six research centers and academic support units report to Dr. Weiss, including the Division of State-of-the-Art Engineering and Telecommunications-Based Education.

Prior to his academic experience, Dr. Weiss was Chemist and Technical Administrator at Color Research Corporation in New York City. He served as consultant for ARPA and the Eastman Kodak Research Laboratories, and on various committees of the American Chemical Society, the National Science Foundation, and the Council for International Exchange of Scholars. He is a founding Director of the Massachusetts Technology Park Corporation.

Dr. Weiss is a physical chemist whose research activities have focussed on photochemistry, photophysics, and molecular quantum mechanics. He is the author or co-author of over eighty articles and papers dealing with these and related topics. Frequently sought as a speaker on research and educational themes, he has served as Sigma Xi Northeast Regional Lecturer and American Chemical Society Tour Lecturer. He has been the recipient of an NSF Senior Postdoctoral Fellowship (Sweden) and a Fulbright Fellowship (Germany). He is a member of the American Chemical Society, the Royal Society of Chemistry (London), the New York Academy of Sciences, the American Society for Photobiology, Sigma Xi, Phi Kappa Phi, Phi Lambda Upsilon, and is a Fellow of the American Institute of Chemists.

Dr. Gerald L. Wilson

Gerald L. Wilson received his Bachelor of Science and Master of Science degrees in Electrical Engineering from the Massachusetts Institute of Technology in 1961 and 1963, respectively, and the Doctoral Degree in Mechanical Engineering from M.I.T. in 1965. He has been a member of the M.I.T. faculty since 1965 and is currently Dean of the School of Engineering and Vannevar Bush Professor of Engineering.

In 1966 he co-founded the Electric Power Systems Engineering Laboratory, an activity at M.I.T. centered on the application of electromechanics and electromagnetics to practical systems. From June 1966 to August 1967 he served as a consultant to the American Electric Power Service Corporation and continued as a part-time consultant for eleven years. On returning to M.I.T. he participated in the development of an electric power engineering education and research program in the School of Engineering. From 1971 through 1982 he was Phillip Sporn Professor of Energy Processing and Director of the Electric Power Systems Engineering Laboratory as it grew to include some ten faculty and staff and forty graduate and undergraduate students. His research involved the development of a physical scale model of a power system, the analysis of transformer saturation effects on extra high voltage transmission Systems, the development of new transmission modeling techniques, the development of a new magnetic circuit breaker, the control of electric power systems under emergency state conditions, the analysis and elimination of audible noise due to corona on transmission systems and the development of superconducting generators. In addition he conducted studies on the design of relay systems, the calculation of electric fields in the presence of complex geometries and dielectrics and the analysis of vacuum circuit breakers using laser interferometry techniques. He is the author or co-author of some thirty publications related to the fields of electromechanics and electric power systems.

From 1978 to 1981 he served as Head of the Department of Electrical Engineering and Computer Science and played a role in the formation of and fund-raising for a major microelectronics research facility at M.I.T.

He has been a consultant to a large range of utilities and manufacturers of electrical equipment. He was appointed as one of three special consultants to the Chairman of the Board of the Consolidated Edison Company as part of an investigation of the 1977 New York City blackout. He serves on the Board of and was one of the co-developers of the Massachusetts Technology Park Corporation. He currently serves on the Board of Directors of three Corporations. He was awarded the IEEE Power Engineering Educator of the Year Award, is fellow of IEEE and is a member of the National Academy of Engineers.

8.5 Glossary

ALUMINUM:
The metal most often used in semiconductor technology to form the interconnects between devices on a chip.

ASSEMBLY:
The sequence of mechanical processes that starts with a chip and ends with a packages integrated circuit suitable for direct electronic applications.

BIPOLAR:
An integrated circuit processing technology employing interacting P/N Junctions.

CHARACTERIZATION:
The complete description of all the pertinent variables pertaining to the normal performance of an integrated circuit.

CHEMICAL VAPOR DEPOSITION:
A process that employs one or more gases to react at the surface of a silicon wafer to form a solid film.

CHIP:
A piece of silicon containing an electronic circuit, often used to refer to a complete integrated circuit.

CLASS 100:
A standard of air cleanliness which allows a maximum of 100 particles of 0.5 micron size to be present in a cubic foot of air.

CLEAN ROOM:
A work area of strictly controlled ambient, imposing stringent standards of temperature, humidity, and airborne particulates.

CMOS:
A semiconductor technology using both PMOS and NMOS transistors in each gate and characterized by a very low power consumption.

CONTAMINATION:
A general term used to describe unwanted material that adversely affects the physical or electrical characteristics of a semiconductor wafer.

CUSTOM INTEGRATED CIRCUIT:
An integrated circuit that requires a full set of specially-designed masks for manufacturing.

DEIONIZED WATER:
High purity water treated to remove all conductive impurities.

DESIGN GROUND RULES:
A series of dimensional constraints imposed upon the design of integrated circuits.

DEVELOPMENT:
A photoresist processing step in which photoresist is removed from areas not defined by the masking and exposure step.

DIE:
A piece of silicon containing a complete circuit prior to packaging in the form of an integrated circuit.

DIE ATTACH:
The process of attaching an individual chip to the interior of an integrated circuit carrier (package).

DIFFUSION:
A process used in semiconductor production which introduces minute amounts of impurities into a material such as silicon or germanium and permits the impurity to spread into the substrate. The process is very dependent on temperature and time.

DOPANT:
An element that alters the conductivity of a semiconductor by contributing either a hole or an electron to the conduction process.

DOPING:
The introduction of an impurity (dopant) into the crystal lattice of a semiconductor to modify its electronic properties - for example, adding boron to silicon to make the material more P-Type.

DRAIN:
Along with the source and gate, one of the three regions of a field-effect transistor.

E-BEAM MASK MAKING:
The use of a focused electron beam to define precise patterns on a photomask.

ETCH:
A process for removing material in a specified area through a chemical reaction.

FEATURE SIZE:
The physical dimensions of various elements of the devices composing an integrated circuit.

FET (Field-Effect R\Transistor):
A transistor consisting of a source, gate and drain, whose action depends on the flow of majority carriers past the gate from source to drain.

FOUNDRY:
A facility that provides integrated circuit manufacturing services, particularly in the area of wafer fabrication.

FULL CUSTOM:
A custom integrated circuit whose entire component layout is tailored for a unique application.

FURNACE:
A piece of equipment containing a resistance heated element and a temperature controller. It is used to maintain a region of constant temperature with a controlled atmosphere for the processing of semiconductor devices.

GATE:
Along with the source and drain, one of the three regions of the field-effect transistor.

GATE ARRAY:
A semicustom integrated circuit that is produced from a standard wafer containing unconnected gates or components; these devices are connected ("personalized") during the final stages of processing to produce the desired circuit.

GEOMETRIES:
A term used to describe the minimum feature size to be employed in the patterning operations of a given process technology.

HEPA:
High efficiency particulate air filtration used to remove microscopic particles from air supplied to clean rooms.

HOLE:
The absence of a valence electron in a semiconductor crystal. Motion of a hole is equivalent to motion of a positive charge.

INTEGRATED CIRCUIT:
A circuit in which many elements are fabricated and interconnected by a single process on a single chip of semiconductor material, as opposed to a "nonintegrated" circuit in which the transistors, diodes, resistors, etc. are fabricated separately and then assembled.

INTERCONNECTION:
The pattern of conductive material (commonly an aluminum alloy) used to provide electrical connection to various components of an integrated circuit chip.

ION:
An atom that has either gained or lost electrons, making it a charged particle (either negative or positive).

ION IMPLANTATION:
Introduction into a semiconductor of selected impurities in controlled regions, via high-voltage ion bombardment, to achieve desired electronic properties.

JUNCTION:
The interface at which the conductivity type of a material changes from P-Type to N-Type or vice versa.

JUNCTION DEPTH:
The depth of a junction in a semiconductor.

MICROLITHOGRAPHY:
Photolithographic processing of images in the sub-micron region.

MICRON:
A unit of length. One micron is one millionth of a meter (10^{-6} meter).

MOS (Metal Oxide Semiconductor):
A semiconductor technology characterized by the employment of field-effect transistors containing a metal gate over thermal oxide over silicon structure.

NMOS:
An MOS technology employing only N-Type structures in an P-Type substrate.

N-TYPE:
A semiconductor material in which the majority of carriers are electrons and therefore negative.

PARAMETRIC:
Adjective describing the measurable characteristics of a device.

PASSIVATION:
Treatment of a region of a device to prevent deterioration of electronic properties through chemical action or corrosion. Usually passivation protects against moisture or contamination. Layers of silicon dioxide or silicon nitride are often used for passivation.

PATTERNING:
The creation of silicon wafers containing geometrical patterns that form electronic components and the connections between them.

PHOTOMASK:
A glass plate covered with an array of patterns used in the photomasking process. Each pattern consists of opaque or clear areas that respectively prevent or allow light or clear areas that respectively prevent or allow light through. The masks are aligned with existing patterns on silicon wafers and used to expose photoresist prior to etching silicon dioxide or a metal.

PHOTORESIST:
A light-sensitive film spun onto wafers and "exposed" using high density light through a mask. The exposed photoresist which allows etching to take place in some areas while preventing it in others.

P/N JUNCTION:
Within a crystal, an interface between a P region that conducts primarily by holes and an N region that conducts primarily by electrons.

PMOS:
An MOS technology employing only P-Type structures in an N-Type substrate.

POLYCRYSTALLINE SILICON:
Silicon composed of many crystals.

PROCESS TECHNOLOGY:
A means of fabricating integrated circuits; process technologies are distinguished by the type of materials used, the physical structure of the circuit, or both.

PROJECTION ALIGNER:
A tool employed to transfer a repeating pattern or image from a photomask to a photoresist layer on a silicon wafer without physical contact between mask and wafer.

PROTOTYPE:
One of an initial batch of integrated circuits produced to confirm the operation of the design.

P-TYPE:
Semiconductor material in which the majority carriers are holes and therefore positive.

REACTIVE ION ETCHING:
A chemical reaction involving ionized gases impinging on an electrically biased substrate.

REACTOR:
A piece of equipment used for the deposition of a layer of material used in semiconductor processing.

REFLOW PLANARIZATION:
A process involving the melting of a glassy film on the surface of a silicon wafer to smooth any sharp contours.

RETICLE:
A glass plate containing a 10X-scale photographic image of a layer of the integrated circuit layout; it is produced by a pattern generator and is used either to produce a photomask or directly in wafer fabrication.

SEMICONDUCTOR:
Crystalline substance (such as silicon) with fewer free electronics than a conductor but more than an insulator, allowing a limited flow of electric current; the conductive properties of a semiconductor are altered by "doping" it with different substances, forming either "N" or "P" type material.

SEMICUSTOM INTEGRATED CIRCUIT:
An integrated circuit that is partially preprocessed, with the number and layout of devices already defined; customization is achieved through the design of the masks that determine the interconnections between components or gates; the most common type is the gate array.

SILICON DIOXIDE:
A passivating layer that can be thermally grown or deposited on silicon wafers. Thermal silicon dioxide is commonly grown using either oxygen (O_2) or water vapor (H_2O) at temperatures above $900^{o}C$.

SILICON NITRIDE:
A passivation layer chemically deposited on wafers at temperatures between 600° and $900^{o}C$. It protects devices against contamination.

SOURCE:
Along with the gate and drain, one of the three regions of a field-effect transistor (FET).

SPUTTERING:
A method of depositing a film of material on a desired object. A target of the desired material is bombarded with ions which knock atoms from the target and deposit them on the object to be coated.

SUBSTRATE:
The underlying material upon which a device or circuit is fabricated.

THERMAL OXIDE:
On silicon semiconductor devices, an oxide fabricated by exposing the silicon to oxygen at high temperatures.

THRESHOLD:
A characteristic voltage at which a field-effect transistor turns on.

TOPOGRAPHY:
The configuration of a surface including verticle reliefs and contours.

VLSI (Very Large Scale Integration):
A level of integrated circuit complexity characterized by several thousands to hundreds of thousands of gates per chip.

WAFER:
A circular piece of silicon, typically 3-6 inches in diameter and 10-20 thousandths of an inch thick; after the fabrication process it contains between several hundred and several thousand individual circuits.

WAFER FABRICATION:
The sequential process of transferring patterns from masks to silicon wafers combined with several high temperature operations, creating individual circuits that are then separated and packaged as integrated circuits.

WAFER SAWING:
The process of separating individual die from an integrated circuit wafer.

WAFER STEPPER:
A tool employed to transfer an image of a single integrated circuit chip pattern directly from a reticle to multiple positions in a photoresist layer in a series of repetitive steps.

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